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A LOW-VOLTAGE TWO-STAGE CMOS OTA WITH ENHANCED DC-GAIN FOR BIOMEDICAL APPLICATIONS

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Abstract: This paper presents the design and analysis of a low supply voltage Second-order OTA-C filter that gives high gain on a large range of frequencies for biomedical applications. Since the performance of the filter strongly depends on the basic building block transconductance cell, a low-power, highly linear, differential transconductance cell working at 1.8V in 180nm CMOS is designed. The proposed configuration uses the technique of cascading transconductance differential amplifier and PMOS common source amplifier to obtain a large gain. This two-stage configuration is designed and simulated by Cadence Virtuoso using Generic Process Design Kit 180nm with a 1.8Volt power supply. The proposed approach makes it possible to enhance the gain, gain bandwidth, and slew rate with a low power dissipation of 67µW.

Keywords: OTA-C filter; Transconductance cell; 180nm CMOS; Differential amplifier; Generic Process Design Kit.

1. Introduction

The electronics industry is moving towards smaller, more portable devices that use less energy, especially in medical applications (Kumngern and Dejhan [7]). Analog circuits are particularly affected by power consumption, so there is a need for circuits that can work at low supply voltage and use minimal power, while still providing high gain and low transconductance. Designing and implementing such circuits is a difficult task for circuit designers. Op-amps were previously utilized for several analog circuit applications. However, due to their high-power consumption and limited frequency capabilities, they have been replaced by Operational Transconductance Amplifiers (OTAs). OTAs are widely used for converting input voltages to output current and play a vital role in numerous analog circuits' applications (Mathad [9]). Hence OTA operates as a voltage-controlled current source.

1.1 OTA overview and available implementations

OTAs are now fundamental components that are used in various modern analog circuits. OTAs are used as a key element in a large variety of circuits that benefit from voltage control. In essence, an OTA is a monolithic direct-coupled differential voltage-controlled current source (DVCCS) with high output impedance (Modi and Patel [10]). Feedback is added to control its overall performance, when operated into a suitable load with provision for feedback, these amplifiers are very well suited for a wide variety of applications. The output current (I out) of OTA is a function of the two input voltages, Vin+ and Vin-. OTA's transconductance can be controlled with a bias current. This is why an OTA is typically used as a high-impedance differential input stage. Also, OTAs are used for precision control of amplifier gain or filter frequency with a relatively wide range (Parveen [11]).

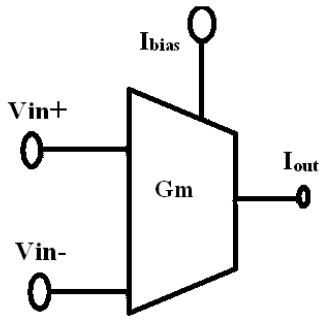

Fig.1. Symbol of OTA

The symbol of OTA is shown in Fig.1. An ideal OTA has two input voltages with infinite input impedance. The function of I_{bias} is to control the amplifier gain. The I_{bias} is proportional to the transconductance (Gm) of OTA (Garradhi et al. [6]). I_{bias} allows for adjusting the transconductance and output current. Use of OTA is possible without feedback. The equation "(1)" provides the OTA's output current.

$$Iout = Gm\ (Vin+ - Vin-) \quad (1)$$

Various types of OTAs are used as amplifiers for low-supply voltage and frequency-based applications in physiological signal acquisition. These include the Telescopic OTA, the Folded-Cascode OTA using the Wilson Current Mirror, the Folded-Cascode OTA using the Cascode Current Mirror, and the Gain-Boosted OTA, etc. (Saidulu et al. [13], Cortes et al. [2], Dammak et al. [3], Ferreira et al. [4], Silveira et al. [14], Li et al. [8]).

The Telescopic OTA offers advantages such as minimal noise and low power consumption. However, it is constrained by limited output signal swing and challenges in shorting input and output. The Folded-Cascode OTA with Wilson mirror also exhibits restricted output swing, but this can be overcome by using a Cascode Current Mirror, which results in higher gain, increased output swing, and good slew rate. However, when designing ultra-low frequency gm−C filters for physiological signals, there is a unique demand for low gm values in the OTA. Lower gm values allow for the use of smaller on-

chip passive components to achieve the desired low filter frequencies. This is particularly relevant in the design of a filter for an ECG signal acquisition setup, where the frequency components range from 0.01 to 300Hz. Designing an Op amp-RC filter for these frequencies would typically require high values of resistances and capacitances, as provided in "(2)".

$$f \alpha gm/C; \text{ since } f \alpha 1/RC \quad (2)$$

An alternative is to utilize the gm-C design technique, which can eliminate passive resistances, resulting in a resistor-less design. Nevertheless, when dealing with moderate to large values of gm, the on-chip capacitor values still need to be significant. Hence, there is a requirement to design an ultra-low gm OTA to enable the realization of ultra-low frequency filters using small-valued on-chip capacitors. The two-stage CMOS OTA is shown in Fig. 2. Stage 1 features a differential amplifier with an input differential pair of NMOS transistors. This configuration is planned to maintain a constant bias current by introducing a current-mirror circuit (Razavi [12]). Stage 2 functions as a common source (CS) amplifier stage, designed to enhance DC gain and maximize the output voltage swing (Gaonkar et al. [13]). The Miller compensating technique is utilized in the high gain stage of an amplifier to maintain stability. (Abdulaziz et al. [1]).

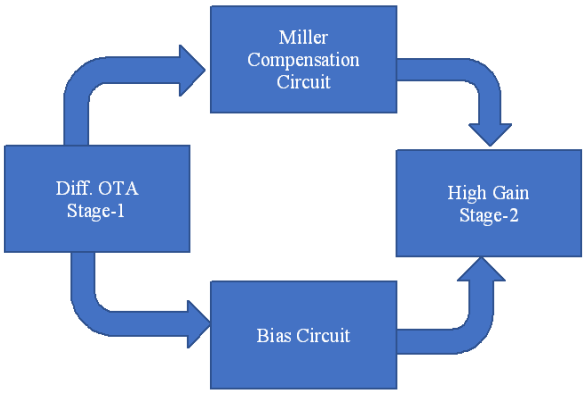

Fig 2: 2-Stage CMOS OTA

2. Two stage OTA

Two-stage OTA circuit schematics is shown in Fig.3. It consists of eight main transistors, each with its specific job. The stage, consisting of transistors M1 and M2, takes voltage signals and converts them into current. Transistors M3, M4, M5, and M8 act as PMOS and NMOS current mirror, while transistors M6 and M7 make up the 2nd-stage amplifier. This setup has the advantage of providing a higher gain because the second stage allow for a greater output voltage swing.

The one stage op-amp allows the small signal current produce by the input pair to flow directly through the output impedance; they perform voltage to current conversion only once. The gain of this topology is therefore limited to product of input pair's

transconductance and output impedance. Hence it observes that cascading in such circuit increase the gain while limiting the output swing.

When we cascade more than two stages, we can achieve higher gain; however, each stage introduces at least one pole in the open-loop transfer function, which can complicate stability assurance in feedback systems employing such op-amps (T.-V. Cao et al. [15]). Therefore, op-amps with more than two stages are seldom utilized (Razavi [12]).

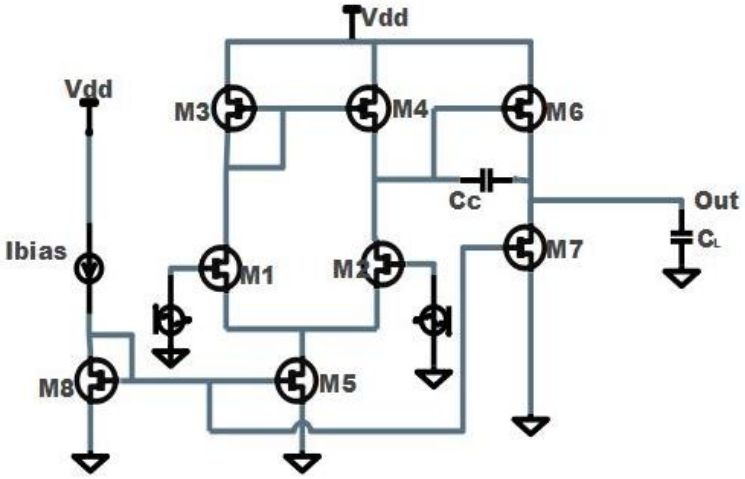

Fig 3: Two Stage CMOS OTA Circuit Schematics

3. Analysis of the Proposed OTA

The proposed OTA design with a combination of a 2-input transconductance amplifier with PMOS common source amplifier, because a differential amplifier does not offer significant gain, so, it is necessary to design a two-stage OTA. The gain of this OTA by small signal analysis is given by equation "(3)". Small signal analysis diagram for gain calculation is shown by Fig. 4.

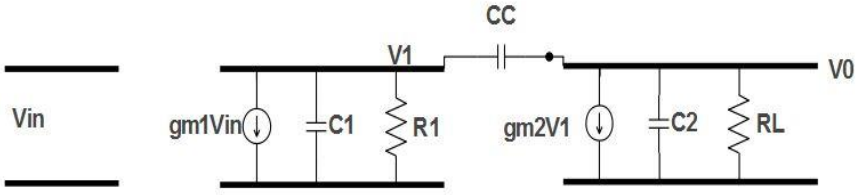

Fig 4: Small Signal diagram of CMOS OTA

$$\frac{V_0}{V_{in}} = \frac{g_{m1}R_1 g_{m2}R_L\left(1-\frac{sC_C}{g_{m2}}\right)}{s^2(\,R_1R_L(\,C_1C_2+C_1C_C+C_2C_C)+s(R_L(C_C+C_2)+R_1(C_C+C_1)+C_CR_1g_{m2}R_L)+1} \quad (4)$$

For two pole system standard equation is given by equation "(4)"

$$\frac{V_0}{V_{in}} = \frac{A_{DC}(1-\frac{s}{z})}{(1-\frac{s}{p_1})(1-\frac{s}{p_2})} \quad (5)$$

By comparing "(3)" with "(4)" poles and zeros are calculated and pole locations are given by "(5)" and "(6)", and zero is given by "(7)".

For two pole system standard equation

$$p_1 = \frac{g_{m1}R_1 g_{m2}R_L(1-\frac{sC_C}{g_{m2}})}{((R_L(C_C+C_2)+R_1(C_C+C_1)+C_C R_1 g_{m2}R_L)} \approx \frac{1}{C_C R_1 g_{m2} R_L} \quad (6)$$

$$p_2 = \frac{g_{m2}C_C}{(C_1C_2+C_1C_C+C_CC_2)} \quad (7)$$

$$p_2 = \frac{g_{m2}C_C}{C_CC_2} = \frac{g_{m2}}{C_2} \quad (8)$$

$$\frac{g_{m2}}{C_L} \quad (9)$$

From above equations, phase calculation

$< \frac{V_O}{V_{in}}$ = -tan$^{-1}(\frac{w}{z})$ -tan$^{-1}(\frac{w}{p_1})$ -tan$^{-1}(\frac{w}{p_2})$

When w= GBW (Gain Bandwidth Product)

$< \frac{V_O}{V_{in}}$ = -tan$^{-1}(\frac{GBW}{z})$ -tan$^{-1}(\frac{GBW}{p_1})$ -tan$^{-1}(\frac{GBW}{p_2})$,

From assumption

z ≥10 GBW

$\frac{g_{m2}}{C_L} \geq 10 \frac{g_{m1}}{C_L}$

$g_{m2} \geq 10 g_{m1}$ (10)

from "(9)" above equation can be written as

$< \frac{V_O}{V_{in}}$ = -tan$^{-1}(\frac{1}{10})$ -tan$^{-1}(A_{DC})$ -tan$^{-1}(\frac{GBW}{p_2})$

-180^0 +PM= -5.71^0 - 90^0 - tan$^{-1}\frac{GBW}{p_2}$)

The Phase Margin (PM) of an OTA should be at least 45° for stability. A greater PM enhances stability but reduces OTA's circuit speed. However, an excessively large PM slows down OTA's circuit speed, while a too small PM can lead to oscillations and stability issues in the circuit.

For 60^0 Phase Margin -

$60^0=84.29^0-\tan^{-1}(\frac{GBW}{p_2})$

$\tan^{-1}(\frac{GBW}{p_2})=24.29$

$\frac{GBW}{p_2}=\tan(24.29)=0.4513$

$p_2= 2.2\ GBW$

From "(6)" putting pole p_2

$\frac{g_{m2}}{C_L}\geq 2.2\ \frac{g_{m1}}{C_C}$

by "(8)"

$10\ \frac{g_{m1}}{C_L}\geq 2.2\ \frac{g_{m1}}{C_C}$

$C_C\geq 0.22\ C_L$

For 2pF load capacitance $C_C\geq 0.44$pF

for designing purpose C_C = 800fF.

4. Calculation of tail current

Slew Rate= I_{SS}/C_L

$I_5=C_L$*Slew Rate = 2pF* 20V/µs=40µA

Hence 20µA for Differential Amplifier Stage 1 and 20µA for CS amplifier Stage 2.

5. Calculation of size of MOS transistors

By the voltage division method voltage at the drain and gate of the $M_{1,2}$ transistor is 0.9V and 0.45V respectively, hence gate voltage across M_1 becomes 1.04V. By parametric analysis, sweeping width 'W' at 10 µA current Width obtains 1.8825µm. Similarly, the M_5 transistor voltage at the drain and gate of the M_5 transistor is 0.45V and 0V; hence gate voltage across M_1 becomes 590mV. By parametric analysis, sweeping width 'W' at 20 µA current Width obtains 3.99µm. Same for M_7 at drain voltage 0.9V, and grounded gate terminal, gate voltage becomes 590mV, by parametric analysis, sweeping width 'W' at 20 µA current Width obtains 3.810µm. For $M_{3,4}$ at 1.8V gate voltage and 0.9V drain and gate voltage, sweeping width 'W' at 10µA Width obtained 922.934nm. Similarly, for M_6 width 'W' at 20 µA Width obtains 1.83121µm. Table 1 shows W/L ratios, Transistor transconductance, and output resistance of each MOS transistor.

Table 1: Aspect ratio, Transconductance, and Output Resistances of the Proposed Design

Transistors	W(µm)/L(µm)	g_m (µA/V)	Rout(Ω)
M_1, M_2	1.8825/0.5	129.157	773.971k
M_3, M_4	0.922/0.5	39.1165	1.5051M
M_5,M8	3.99/0.5	263.06	394.612k
M_6	1.831/0.5	78.479	770.33k
M_7	3.810/0.5	260.6	622.769k

6. Modifications to enhance the performance of the OTA circuit

- Reducing the size of MOS transistors in two stages OTA circuit, because it consumes low power (83% reduction in total power consumption as compared to the reference circuit by Gaonkar *et al.* in [13]). Hence battery life in biomedical filters, which are designed with a small aspect ratio of two stages OTA, is increased.
- Since, smaller transistors generate less heat, which can make it easier to manage thermal issues in high-performance devices (Vittoz [16]). Hence Heat dissipation of the two-stage OTA circuit is improved.
- This circuit schematic is designed using a single supply voltage V_{DD}. To achieve higher gain, by changing the size of MOS transistor, the output resistance of the stage-2 amplifier increased to 770.33k Ω from 485.026 Ω and transconductance decreased to 78.479µA/V from 1.28798µA/V (in comparison with reference circuit). The aim to reduce transconductance is to reduce distortion in the output signal, by this linearity of circuit increase and power consumption decrease. By small transconductance OTA circuit, compensation becomes easier, so 800fF capacitor is used rather than 3pF used in reference circuit. Small-size capacitors require a small area, hence this OTA circuit requires a small chip area.

7. Simulation Result

The proposed OTA is simulated using Cadence Virtuoso 180nm CMOS technology. AC response of OTA is shown in Fig. 5. Similarly, Fig. 6 and 7 show the transient response curves of the input and output signals, respectively. The peak-to-peak values of the output and input signals are 1.507V and 2mV, as obtained from the transient analysis curve. The DC gain of OTA is 70.9dB, phase margin 60^0 and -3dB frequency at 67.9 dB gain 12.81 kHz, zero dB frequency is 23.19MHz. The transient Power analysis curve is shown in Fig.8. From the Transient power analysis curve total power consumption of OTA found to be ≈ 67 µW.

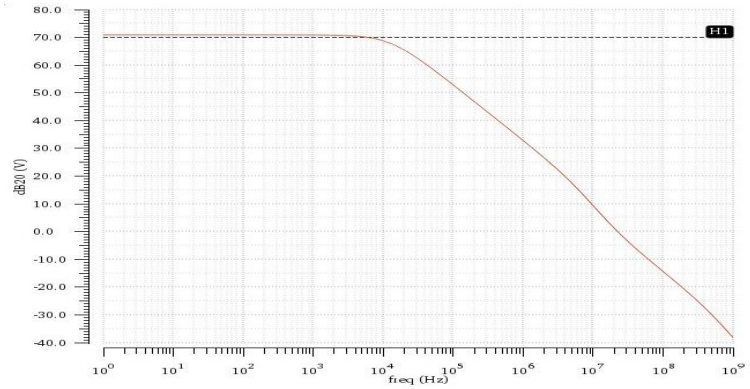

Fig. 5: AC analysis curve

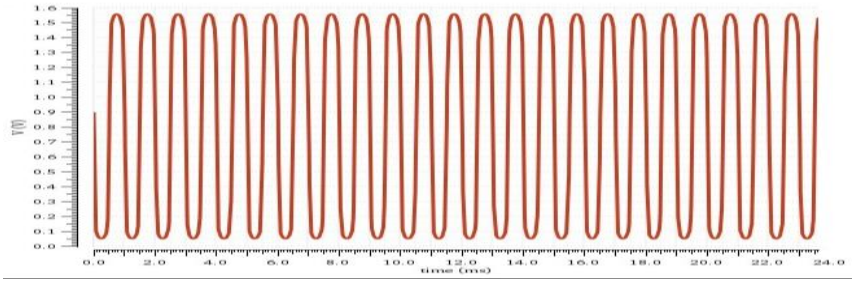

Fig. 6: Transient analysis output response curve

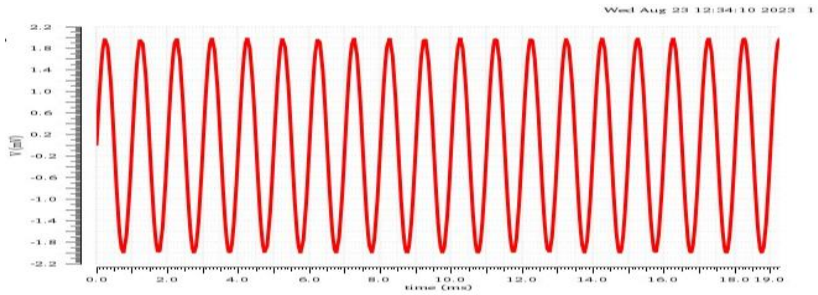

Fig 7.: Transient analysis curve of input response

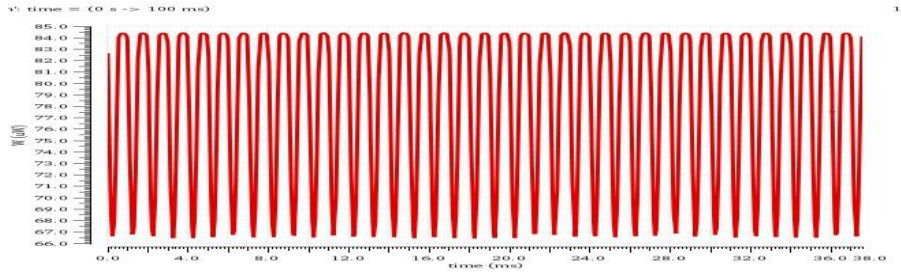

Fig 8: Transient power analysis

Higher gain and higher bandwidth can be obtained by increasing the size of the transistor of M_1 and M_2. Transistors M_3 and M_4 control maximum ICMR (Input Common Mode Range), and M_5 control minimum ICMR. Coupling Capacitor does not affect gain, but it directly affects Gain Bandwidth. For a high slew rate, a high value of coupling capacitor Cc is required.

8. Summary of the proposed circuit and performance comparison

Table 2 shows the characteristics results of the 2-stage OTA circuit simulation, with a performance comparison of related work.

Table 2: Performance Summary

Specification	Proposed Work	Ref. [13]
Technology(μm)	0.18	0.18
Supply Voltage	1.8V	2.5V
DC Gain	70.9dB	46.5dB
UGBW (Unity Gain Band Width)	23.19 MHz	9.9 MHz
Phase Margin	60^0	75^0
Slew Rate	20V/μs	3.2V/μs
CMRR (Common Mode Rejection Ratio)	97dB	96dB
Power Dissipation	67μW	403μW

9. Conclusion

The two-stage OTA that operates with a 1.8V power supply has been designed for the use of biomedical sensor interface. Power and voltage are important factors in designing analog and mixed-mode signals and systems. This paper discusses the design, implementation, and simulation of a two-stage gate-driven OTA with high CMRR using 180nm CMOS technology. Simulation results show a DC gain of 70.9 dB, PM of 60^0, Slew Rate of 20V/μs, CMRR of 97dB, and Power Dissipation of 67μW.

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