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SZIKLAI PAIR AND DARLINGTON PAIR RTL INVERTERS FOR HIGH DRIVE CURRENT APPLICATIONS

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Abstract: As a novel approach, two different single-input RTL inverter (NOT gate) circuits using Sziklai and Darlington pairs are developed and qualitatively analyzed in the present manuscript. Performance of the proposed inverters are also compared with the conventional RTL inverter circuit. Respective inverter circuits use default PSpice models of NPN and PNP BJTs to constitute switching devices. Proposed inverters produce high drive current, full output swing, high static-noise-margin (SNM), low input current along with nearly ideal switching threshold voltage for Sziklai pair RTL inverter. Problem of low-drive current and low static-noise-margin of the conventional CMOS and TTL based inverters are also addressed in the manuscript. Respective outcomes strongly justify the idea of using Sziklai pair and Darlington pair RTL inverters for high drive current applications.

Keywords: Sziklai pair; Darlington pair; single-input RTL inverter; drive current; output swing.

1. Introduction

Very-large-scale integration (VLSI) technologies have seen an evolution from deep-submicron level to nanoscale hybrid level integrating nano CMOS devices [1,2,3]. As the CMOS technology is scaled down to improve the performance, the design of low-power, low-voltage, and high-speed VLSI devices is found to be affected by the process parameter variations and therefore designing low-power digital VLSI device is a big challenge for VLSI designers [3,28,10,27].

In addition, the anticipation of high speed, ultra-low power in digital VLSI circuits has necessitated a new design methodology, that is, to apply digital VLSI circuits to analog VLSI systems to acquire a better level of performance [7]. Analog VLSI design is very useful because it requires a small number of transistors for a wide range of applications, thus a large network can be built on a single chip [7,9]. Despite having many advantages, it also suffers from traditional challenges such as accurate component values, device matching, the impact of the layout in the design, reliability of IC, use of mixed-signal verification methodology, and Noise analysis [31,17,12].

A number of approaches, available with the VLSI designers, show that when the NOT gate is applied on a Digital or Analog VLSI system in smaller geometry, they give low

drive current and insufficient output voltage swing [6,5,14,18,25,18]. In this reference the investigations of Nosratinia et. al. to develop a high-swing, high-drive CMOS buffer [6], Park et al [5] to introduce a new model for estimating effective drive-current in CMOS inverter for sub-45nm technology, Mukhopadhyay et al [14] to design a nanoscale CMOS inverter with symmetric switching characteristics M.H. Na et al. [18] to deduce the expression for effective drive-current of CMOS inverter, Woorham Bae [15] to describe recent achievements on utilizing a COMS inverter as an analog circuit and Sarnago et al [16] to introduce an optimized base drive circuit for SiC- BJT based series resonant inverter are worth mentioning.

Compensating the technical gap, the present investigation effectively introduces two different designs of Sziklai pair and Darlington pair RTL inverters having much higher drive currents than CMOS and TTL based ICs [29]. In addition to it, proposed inverters also produce high Static-Noise-Margin in comparison to other popular VLSI technologies [16]. As a special feature, the proposed RTL inverter with Sziklai pair holds a switching threshold voltage almost nearer to the ideal requirement.

It is to note that Sziklai pair consists of two BJTs of opposite polarity with collector of the first BJT drives the base of the second whereas Darlington pair holds two BJTs of the same polarity with emitter of the first BJT drives the base of the second [29]. In recent years, the Sziklai pair is being preferred over Darlington pair due to its unique feature that its base turn-on voltage (~625mV) is half as compared to the Darlington pair (~1.36 Volts) [16]. Sziklai pair has also better thermal stability due to lower heat dissipation as compared to the Darlington pair. However, due to small amount of in-built negative feedback, its current gain factor ($\beta_{Q1}\beta_{Q2}+\beta_{Q1}$) is slightly less than that of the Darlington pair ($\beta_{Q1}\beta_{Q2}+\beta_{Q1}+\beta_{Q2}$) but is approximated to be equal at higher β values [32,23]. Tewari and Saraswati [24] on energy efficient coverage and Prakash et al. [25] on arresting the complex growth rate of perturbation discussed.

In the last decade, Sziklai pair became instrumental in designing power amplifiers whereas its use to develop small-signal amplifiers have also attracted attention of researchers [29,16,32,23,19]. However, the use of Sziklai pair and Darlington pair in the area of digital electronics is still the domain of curiosity for researchers and electronic circuit designers. Thus, in the present manuscript, an attempt is made to develop and study the performance of two RTL inverters (NOT gate) using Darlington pair and Sziklai pair respectively. The findings are also compared with the conventional RTL inverter.

2. Circuit Description

Circuit idea of the Conventional BJT led RTL inverter along with proposed Darlington pair RTL inverter and Sziklai pair RTL inverter, are illustrated in Fig. 1.

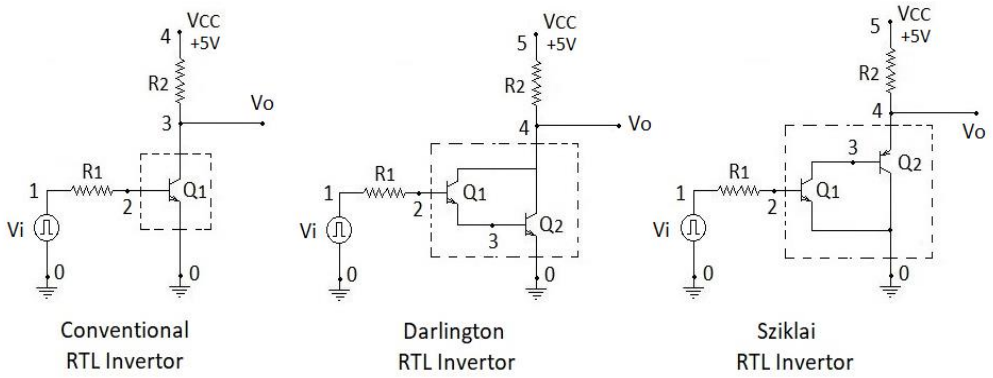

Fig.1: Illustrating the Circuit Idea of Conventional RTL inverter, Darlington pair RTL Inverter and Sziklai pair RTL Inverter

Conventional RTL inverter in Fig. 1 is included in the discussion as reference circuit. This helps to bring a comparative study of the established and the proposed circuit of RTL inverters. Respective inverters use common-emitter RTL configuration in their circuit design. Circuit configuration of these inverters employ base resistance (R_1) connected between input pulse and base terminal whereas collector resistance (R_2) is joined between collector terminal and the DC biasing supply. Base resistance is generally consumed for converting an input voltage into current whereas collector resistance is used for converting collector current into voltage [18].

Refer to Fig. 1. Device structure of Sziklai pair RTL inverter uses NPN transistor 'Qbreakn' at driver position and PNP transistor 'Qbreakp' at follower position, therefore, the respective device is referred as NPN Sziklai pair [26]. Similarly, the Darlington pair RTL inverter uses NPN BJT 'Qbreakn' at both driver and follower positions in the device configuration, and hence the respective device is referred as NPN Darlington pair [26].

All the three inverters under discussion use the default PSpice model of BJTs with a nomenclature Qbreakn (β=100) to represent NPN and Qbreakp (β=100) to refer PNP type bipolar junction transistors [26]. As usual every inverter is biased with +5 Volt DC Supply voltage. Observations are recorded with the aid of PSpice simulation software by feeding the respective inverters with input pulse of the period 60 Nano Seconds [26]. It is to note that the parametric specification to define Input Pulse Source for the inverters under discussion holds Input Voltage V1=0V, Pulsed Voltage V2=5V, Delay Time TD=1 Nano Seconds, Rise Time TR=1 Nano Seconds, Fall Time TF=1 Nano Seconds, Pulse width PW=38 Nano Seconds and Period PER= 60 Nano Seconds.

Statements of circuital components containing active and passive elements are depicted in Table 1 whereas model parameter and operating point details are briefed in Table 2 and Table 3 respectively.

Table 1. Component Details of the Respective RTL Inverters

Description of Circuit Components	**Conventional RTL Inverter**	**Sziklai RTL Inverter**	**Darlington RTL Inverter**
Q1 (First Transistor)	Qbreakn	Qbreakn	Qbreakn
Q2 (Second Transistor)	NA	Qbreakp	Qbreakn
R_1 (Source/Base Resistance)	30Ω	5 K Ω	1Ω
R_2 (Collector Resistance)	1Ω	1 Ω	1 Ω
V_{CC} (DC Biasing Supply)	±5 Volt	±5 Volt	±5 Volt
V_{IN} (Input Pulse Source)(V1 V2 TD TR TF PW PER)	0 5 1NS 1NS 1NS 38NS 60NS	0 5 1NS 1NS 1NS 38NS 60NS	0 5 1NS 1NS 1NS 38NS 60NS

Table 2. Model Parameters for BJTs in the Device Structure of Respective RTL Inverters

Model Parameters	**Qbreakn**	**Qbreakp**
IS (p-n saturation current)	100 atto Amp	100 atto Amp
BF (Ideal Maximum forward Voltage)	100	100
BR (Ideal Max reverse beta)	1	1
NF (Forward Current Emission Coefficient)	1	1
NR (Reverse Current Emission Coefficient)	1	1
CN (Base Collector leakage emission Coefficient)	2.42	2.2
D (Diode)	.52	.87

Records in Table 3 depicts the major operating parameters of the BJTs received after the simulation of the respective circuits. Values corresponding to IB (Current Flowing into base), IC (Current flowing into collector), VBE (Voltage across base-emitter junction), VBC (Voltage across base-collector junction, VCE (Voltage across collector emitter junction), BETA DC (Small Signal DC Current gain), GM (Small Signal Transconductance), RPI (Small Signal AC Base Emitter Resistance), RO (Small Signal AC collector emitter resistance) and BETA AC (Small-signal AC Current gain) clearly indicates the effective participation of BJTs in respective inverter circuits.

Table 3. Description of Effective Operating Parameters of Respective RTL Inverters

Operating Point Parameters	Conventional RTL Inverter	Sziklai RTL Inverter		Darlington RTL Inverter	
	Qbreakn NPN	Qbreakp PNP	Qbreakn NPN	Qbreakn NPN	Qbreakn NPN
IB	-5.0 pA	-9.15 pA	-4.58 pA	-5.01 pA	4.26 pA
IC	0.1 pA	-1.38 µA	9.15 pA	9.27 pA	86.1 nA
VBE	15.0 nV	-42.5 V	.229 nV	-73.2 V	73.2 V
VBC	-5.00 V	4.57 V	-4.57 V	-5.00 V	-4.27 V
VCE	5.00 V	-5.00 V	4.57 V	4.27 V	5.00 V
BETA DC	-2.00	151	-2.00	-1.85	202.0
GM	3870.0pA/V	0.531nA/V	3870.0pA/V	0.00	0.531nA/V
RPI	.996 TΩ	1.89 GΩ	.996 TΩ	.1 PΩ	1.75 GΩ
RO	1.00 GΩ	1.00 GΩ	1.00 GΩ	1.00 GΩ	1.00 GΩ
BETA AC	38.5	0.01	38.5	0.00	0.01

3. Results and Discussions

3.1 Output Swing

The waveform of input and output pulses of all the three inverters are depicted in Fig. 2, Fig. 3, Fig. 4 and Fig. 5. Respective figures show that output waveforms of all the three inverters produce full output voltage swing of 5 Volt.

It has been observed that on applying the input pulse of range 0 volts to 5 volts and under the pre-concerted values of circuital parameters, Conventional RTL inverter with NPN transistor generates output pulse ranging from 0.106 volts to 5 volts whereas Sziklai pair and Darlington pair RTL inverters produce output pulses ranging from 1.1045 volts to 5 volts and 1.003 volts to 5 volts respectively.

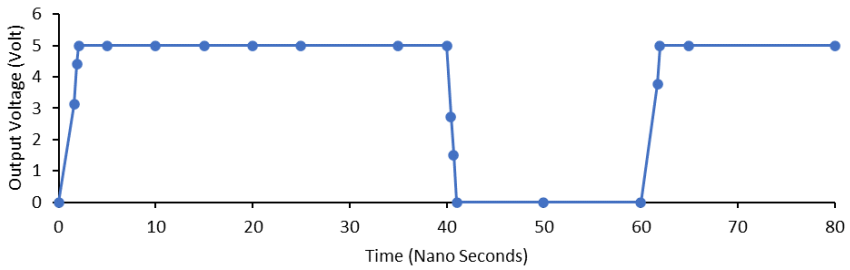

Fig. 2. Input Pulse to the Inverters under discussion

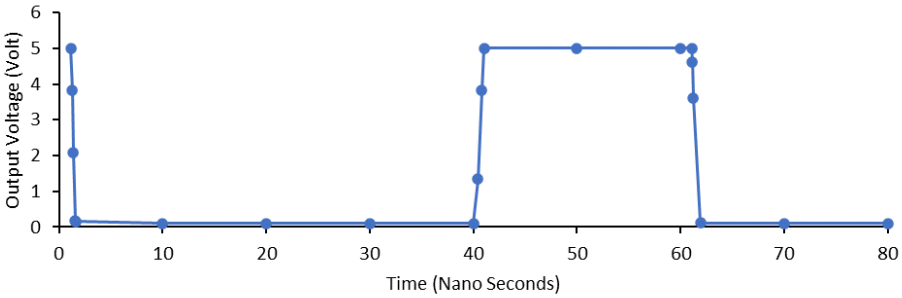

Fig. 3. Output Pulse for Conventional RTL Invertor

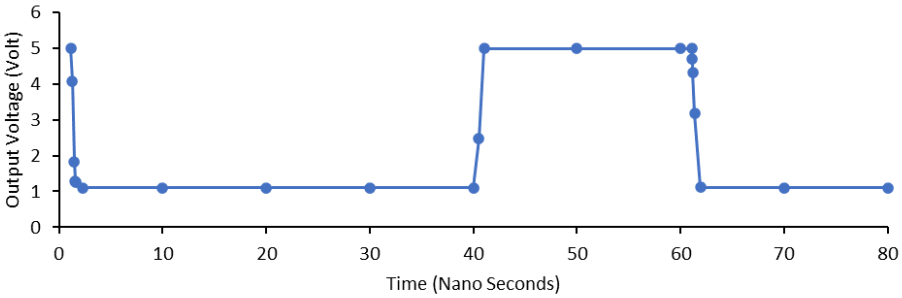

Fig. 4. Output Pulse of Sziklai Invertor

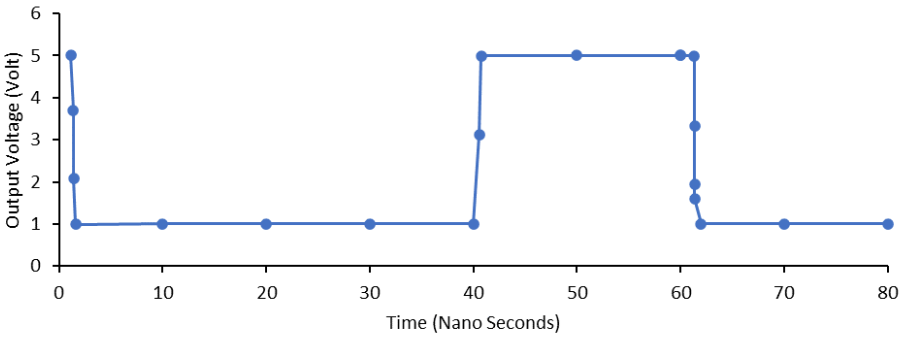

Fig. 5. Output Pulse of Darlington Inverter

It is noteworthy that the range of output pulse of all the three Inverters has a linear proportionality relationship with DC supply voltage, i.e., the range of output pulse increases with increasing value of DC supply voltage. Correspondingly, lowering the supply voltage causes shortening of the range of output pulse [25,3].

3.2 Output Drive Current

The output drive current is an important parameter that elaborates the significance of the design of a digital circuit [5,18]. It is a parameter that designates the amount of current that a single pin of an IC or single terminal of BJT in NOT gate can sink or source [5,18].

It has been observed that CMOS and TTL based ICs produces drive current in the range 4mA-24mA [29], but in the present investigation, it is found that the conventional RTL inverter as well as Sziklai pair and Darlington pair RTL inverters produce comparably high output drive current ranging in 3-5Amp at 5 Volt DC biasing supply. Table 4 shows the typical output drive current of CMOS and TTL based ICs and its comparison with respective RTL inverters of Fig. 1.

Table 4. A Comparison of the Output Drive Currents of Different Devices

Device	Logic Units	Output Drive Current
CMOS	Raspberry Pi GPIO	16 mA
	74HC	4 mA
	AC/ACT/ACQ/ACTQ	24 mA
	4000 Series	4 mA
TTL	TTL (Standard)	16 mA
	Schottky (S)	20 mA
	LPS	8 mA
	ALPS	8 mA
	High Speed	20 mA
	Low power	3.6 mA
RTL	Conventional RTL Inverter	4.8400 Amp
	Sziklai pair RTL Inverter	3.8434 Amp
	Darlington pair RTL Inverter	3.9976 Amp

In addition, variation of output current (I_{OUT}) with respect to the input voltage (V_{IN}) is depicted in Fig. 6. It is observed that the output current of respective inverters (Fig. 1) initially increases with increasing value of input voltage and finally acquires the state of saturation at a critical value of V_{IN}. The output current in conventional RTL inverter occupies saturation trend at a critical input voltage V_{IN}=2.752V (I_{OUT}=4.840Amp). However, Sziklai pair RTL inverter receives saturation in output current at V_{IN}=3.052V (I_{OUT}=3.843Amp) whereas Darlington pair RTL Inverter occupies saturation tendency in I_{OUT} at V_{IN}=1.939V (I_{OUT}=3.997Amp).

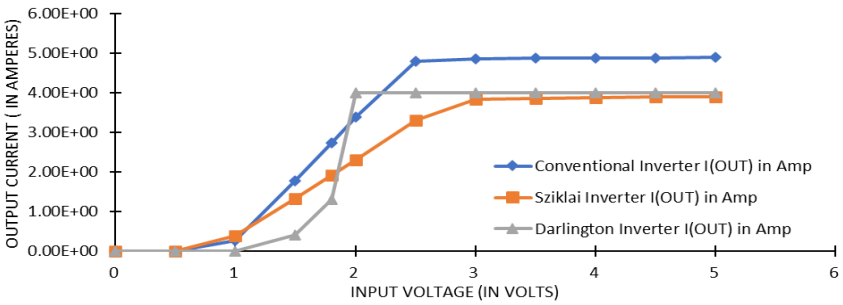

Fig. 6. Variation of Output Current with Input Voltage

It is also to note that the output current of all the three Inverters under discussion strongly depends on DC supply voltage. In other words, increasing DC supply voltage causes a corresponding increase in output current whereas reduction in DC supply voltage causes a decrement in output current in a disparate manner [24].

3.3 VTC Curve and Switching Behaviour

Generally, quality performance of an inverter is measured with the help of Voltage Transfer Characteristic (VTC) curve (Static Characteristic curve) which describes the distribution of output voltage with respect to the input voltage [30]. The VTC curves for the inverters under discussion are sketched in Fig. 7.

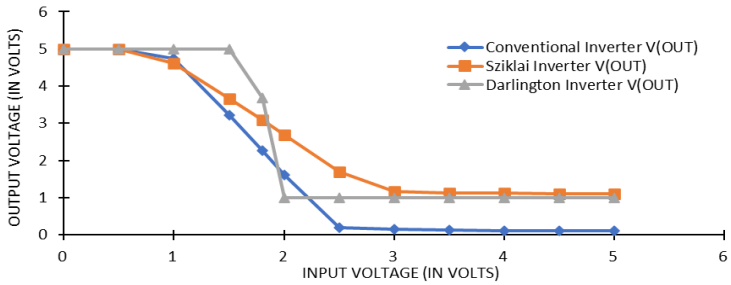

Fig. 7. Voltage Transfer Characteristic Curve

Narration of the methodology to identify the important parameters used for describing the switching behaviour of an inverter is depicted into the VTC curve of the Sziklai pair RTL inverter in Fig. 8. The Fig. 8, quoted as an example, marks the terms V_{OH} (Output High Voltage), V_{IH} (Input High Voltage), V_{OL} (Output Low Voltage), V_{IL} (Input Low Voltage) and various Slops of the VTC curve with an idea to find V_M (Mid-Point Voltage) graphically.

It is to note that the slope of transition region determines the basic switching nature of inverter [30]. Steep slope describes precise switching whereas shallow slope shows switching with higher rise and fall time [14,30]. It is quite apparent from the VTC curves in Fig. 7 and the graphical description in Fig. 8 that the slope of transition regions of Sziklai pair and Darlington pair RTL Inverters are much steeper in comparison to the conventional RTL inverter which, therefore, indicates precise switching nature of the Sziklai and Darlington inverters.

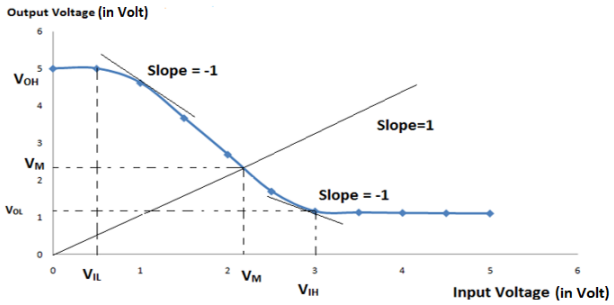

Fig. 8. Depicting general parametric terms used in VTC Curve of Sziklai RTL Inverter

It is noteworthy that inverter resistors play an important role in determining the slope as well as transition region in the VTC curve. Small variation in resistance value causes shifting the curve towards higher input voltage region and trans-positioning the slope of the transition region.

Based on the VTC curve of Fig. 7 and the idea described in Fig. 8, the input low voltage V_{IL}, output high voltage V_{OH}, input high voltage V_{IH} and output low voltage V_{OL} for all the three inverters are computed and respective records are summarized in Table 5.

Table 5: V_{IL}, V_{OH}, V_{IH} and V_{OL} for Respective Inverters

Inverters	**V_{IL}**	**V_{OH}**	**V_{IH}**	**V_{OL}**
Conventional RTL Inverter	0.699 volts	5 volts	2.4 volts	0.312 volts
Sziklai Pair RTL Inverter	0.579 volts	5 volts	2.8000 volts	1.2002 volts
Darlington Pair RTL Inverter	1.2781 volts	5 volts	1.8786 volts	1.0244 volts

Refer to Table 5. Sziklai pair RTL inverter generates high output voltage (V_{OH}=5V) at a very low input voltage (V_{IL}=0.579V) in comparison to conventional RTL inverter (V_{IL}= 0.699V) and Darlington pair RTL Inverter (V_{IL}=1.2781V). However, its output voltage (V_{OL}=1.2002V) tapers off at an input voltage (V_{IH}=2.80V) higher than both conventional RTL inverter (V_{IH}=2.4V) and Darlington pair RTL inverter (V_{IH}=1.8786V). Similarly, Darlington pair RTL inverter produces high output voltage (V_{OH}=5V) at an input voltage (V_{IL}=1.2781V) higher than both conventional RTL inverter (V_{IL}=0.699V) and Sziklai pair RTL inverters (V_{IL}=0.579V) whereas its output voltage (V_{OL}=1.0244V) subsides at an input voltage (V_{IH}=1.8786V) lower than both conventional RTL inverter (V_{IH}=2.4V) and Sziklai pair RTL inverter (V_{IH} =2.80V). This shows the precise-switching nature of Sziklai and Darlington Pair RTL inverters between ON-OFF state.

Cut-off, active and saturation regions of the inverters under discussion has also been computed from the VTC curve and respective data are enlisted in Table 6.

Table 6: Region of Activity for Respective Inverters

Inverters	**Region of Activity (Measured in Volts)**		
	Cut-off Region	**Active Region**	**Saturation Region**
Conventional RTL Inverter	$V_{IN} \leq 0.699$ ($V_{OUT} \geq 5.0$)	$0.699 \leq V_{IN} \leq 2.4$ ($5.0 \geq V_{OUT} \geq 0.312$)	$V_{IN} \geq 2.4$ ($V_{OUT} \geq 0.312$)
Sziklai pair RTL Inverter	$V_{IN} \leq 0.579$ ($V_{OUT} \geq 5.0$)	$0.579 \leq V_{IN} \leq 2.80$ ($5.0 \geq V_{OUT} \geq 1.2002$)	$V_{IN} \geq 2.80$ ($V_{OUT} \geq 1.2002$)
Darlington pair RTL Inverter	$V_{IN} \leq 1.2781$ ($V_{OUT} \geq 5.0$)	$1.2781 \leq V_{IN} \leq 1.0244$ ($5.0 \geq V_{OUT} \geq 1.2786$)	$V_{IN} \geq 1.0244$ ($V_{OUT} \geq 1.2786$)

Refer to Table 6 and Fig. 7. The transition for conventional RTL inverter takes place from high-state V_{OUT} =5V at an input voltage V_{IN}=0.699V. Hence, the Cut-off region for conventional RTL Inverter exist for $V_{IN} \leq 0.699V$ ($V_{OUT} \geq 5.0V$). At an input voltage of V_{IN} = 0.699V, the transition starts and occurs up to an output voltage V_{OUT}=0.312V.

Therefore, an active region exists for an input voltage of range $0.699V \leq V_{IN} \leq 2.4V$ ($5.0V \leq V_{OUT} \leq 0.312V$). At $V_{IN} \geq 2.4V$ ($V_{OUT} \geq 0.312V$), output voltage acquires a saturation tendency. Hence, the input voltage range of the saturation region exists for $V_{IN} \geq 2.4V$**.** Similarly, for the Sziklai pair and Darlington pair-based RTL inverter cut-off regions fall at $V_{IN} \leq 0.579V$ ($V_{OUT} \leq 5.0V$) and $V_{IN} \leq 1.2781V$ ($V_{OUT} \leq 5.0V$) respectively. The range of active region for both Inverters exists at $0.579V \leq V_{IN} \leq 2.80V$ ($5.0V \leq V_{OUT} \leq 1.2002V$) and $1.2781V \leq V_{IN} \leq 1.0244V$ ($5.0V \leq V_{OUT} \leq 1.2786V$) respectively. At $V_{IN} \geq 2.80V$ ($V_{OUT} \geq 1.2002V$), the output voltage of Sziklai pair-based RTL inverter acquires a saturation tendency whereas saturation region for Darlington pair-based RTL inverter exists for the range $V_{IN} \geq 1.0244V$ ($V_{OUT} \geq 1.2786V$).

3.4 Switching Threshold Voltage

The idea to identify the Switching Threshold Voltage graphically is already depicted in Fig. 8. Switching Threshold Voltage is a point on a VTC curve where the output voltage (V_{OUT}) becomes equal to that of the input voltage (V_{IN}) [31]. This particular point is also referred as Mid-point Voltage (V_M). An ideal inverter is one in which the Switching Threshold Voltage (V_M) is found half of the DC biasing voltage of the circuit.

Applying similar philosophy of Fig. 8 on Conventional, Sziklai pair and Darlington pair RTL inverters, the Switching Threshold Voltages of respective inverters are computed and the records are listed in Table 7.

Table 7: Switching Threshold Voltage of Respective RTL Inverters

Inverter	**DC Supply (V_{CC})**	**Ideal Requirement ($V_{CC}/2$)**	**Switching Threshold Voltage (V_M)**
Conventional RTL Inverter	5.00 V	2.50 V	1.093 V
Sziklai pair RTL Inverter	5.00 V	2.50 V	2.2308 V
Darlington pair RTL Inverter	5.00 V	2.50 V	1.8454 V

Table 7 unveil that only Sziklai pair RTL inverter holds a Switching Threshold Voltage nearer to half of the DC biasing Supply of the circuit whereas Darlington pair inverter has a better value of V_M than Conventional RTL inverter. This brings a reasonable possibility for the proposed Sziklai pair and Darlington pair RTL inverters to be a good alternative of the conventional RTL Inverter in digital circuits.

3.5 Static Noise Margin

Static Noise Margin (SNM) determines how immune the inverter is with respect to the noise in terms of voltage. It is generally estimated using "Butterfly Method" in which butterfly-like structure is obtained by plotting the VTC curve with V_{OUT} as a function of V_{IN} and inverse VTC with V_{IN} as a function of V_{OUT} [30,32]. The intersection of both the curve gives two lobes which are used to determine NM_H (High Noise Margin) and NM_L (Low Noise Margin). Respective Butterfly Curves for the Conventional, Sziklai pair and Darlington pair RTL inverters are depicted in Fig. 9, Fig. 10 and Fig. 11.

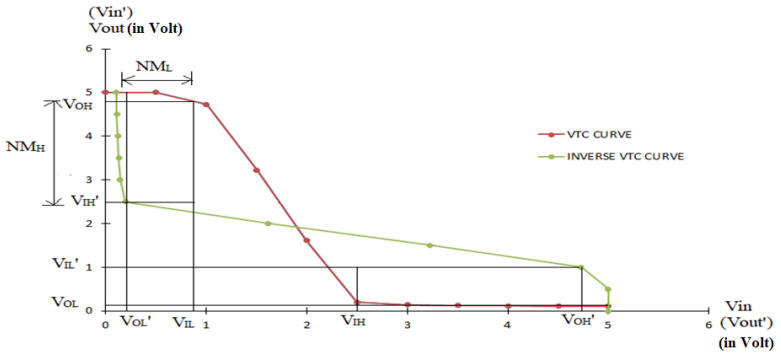

Fig. 9: Butterfly Curve for Conventional RTL Inverter

The Static Noise Margin (SNM) of the respective inverters, with the help of Butterfly Curves, is measured using following expression –

$$SNM = \sqrt{(NM_L)^2 + (NM_H)^2} \quad (1)$$

Where $NM_L = V_{IL} - V_{OL}'$ and $NM_H = V_{OH} - V_{IH}'$

V_{IL} = input low voltage of VTC curve and V_{OH} = output high voltage of VTC curve V_{OL}' = output low voltage of inverse VTC curve and V_{OH}' = output high voltage of inverse VTC curve

It is to be noted that 'Graphical method' has been used here to Calculate SNM for the inverters under discussion [32].

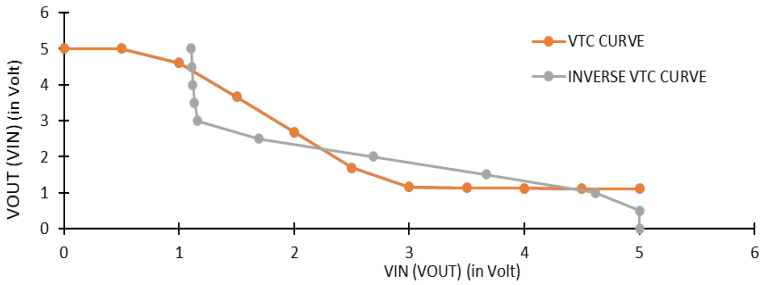

Fig. 10: Butterfly Curve for Sziklai pair RTL inverter

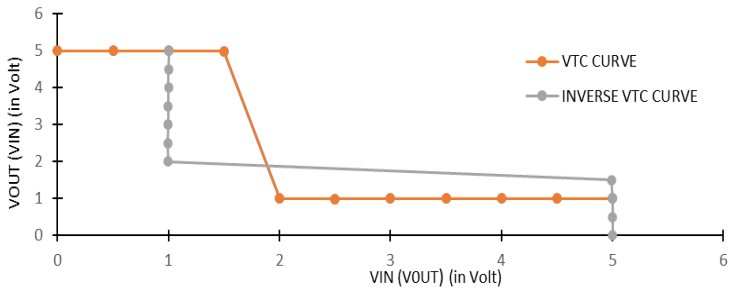

Fig. 11: Butterfly Curve for Darlington pair RTL inverter

Fig. 9 also depicts how to identify the precise values of V_{IL}, V_{OL}', V_{IH}', and V_{OH} for an inverter with the help of Butterfly Curve. Applying similar technique for other inverters, the precise values of V_{IL}, V_{OL}', V_{IH}', and V_{OH} are computed and, thereby respective values of Static Noise Margin are listed in Table 8.

Table 8: Static Noise Margin for the Respective Inverters (Measured in Volts)

Inverters	**V_{IL}**	**V_{OL}'**	**V_{IH}'**	**V_{OH}**	**NM_L**	**NM_H**	**SNM**
Conventional Inverter	0.699	0.199	2.5	5.0	0.5	2.5 V	2.54
Sziklai Inverter	0.579	1.1615	3.0	5.0	(-)0.5825	2.0 V	2.083
Darlington Inverter	1.2781	0.9973	2.0	5.0	0.2808	3.0 V	3.013

A quick comparison of the SNM of respective inverters under discussion with other available technologies are also recorded in Table 9 in which V_{CC} represents the DC biasing voltage of the inverter.

Table 9: Comparison of the Static Noise Margin of various Technologies

Technology	**Measured in Volts**								
	V_{CC}	**V_{OH}**	**V_{IH}**	**V_{TH}**	**V_{IL}**	**V_{OL}**	**NM_H**	**NM_L**	**SNM**
5V-CMOS	5.00	4.44	3.50	2.50	1.50	0.50	0.94	1.00	1.3724
5V-TTL	5.00	2.40	2.00	1.50	0.80	0.40	0.40	0.40	0.5656
3.3V LVTTL	3.30	2.40	2.00	1.50	0.80	0.40	0.40	0.40	0.5656
2.5V-CMOS	2.50	2.00	1.70	1.20	0.70	0.40	0.30	0.30	0.4242
1.8V-CMOS	1.80	1.45	1.20	0.90	0.65	0.45	0.25	0.20	0.3200
5V- RTL	5.00	5.00	2.50	1.093	0.699	0.199	2.50	0.5	2.540
5V-RTL SZIKLAI	5.00	5.00	3.00	2.2308	0.579	1.1615	2.00	(-) 0.58	2.083
5V-RTL DARLINGTON	5.00	5.00	2.00	1.8454	1.2781	0.9973	3.00	0.2808	3.013

Refer to Table 9. It is found that proposed inverters produce high Static Noise Margin (SNM) in comparison to the other popular technologies listed herein [16,32].

3.6 Variation of Output Pulse Range with Input Pulse Range

Variation of output pulse range with respect to input pulse range for all the three inverters are also observed and respective records are enlisted in Table 10.

Table 10: Variation of Output Pulse range with respect to the Input Pulse range

Input Pulse Range (Volts)	Output Pulse Range (Volts)		
	Conventional RTL Inverter	Sziklai pair RTL Inverter	Darlington pair RTL Inverter
0.00 – 0.40	Not Inverted	Not Inverted	Not Inverted
0.00 – 0.50	Not Inverted	4.999997 – 5.00	Not Inverted
0.00 – 0.60	4.999 – 5.00	4.9980 – 5.00	Not Inverted
0.00 – 0.80	4.997 – 5.00	4.9293 – 5.00	Not Inverted
0.00 – 1.00	4.730 – 5.00	4.6140 – 5.00	4.9999995 – 5.00
0.00 – 1.20	4.160 – 5.00	4.2520 – 5.00	4.99998 – 5.00
0.00 – 1.50	3.220 – 5.00	3.6686 – 5.00	4.996 – 5.00
0.00 – 2.00	1.610 – 5.00	2.6875 – 5.00	0.997 – 5.00
0.00 – 2.50	0.199 – 5.00	1.6961 – 5.00	0.993 – 5.00
0.00 – 3.00	0.145 – 5.00	1.1615 – 5.00	0.995 – 5.00
0.00 – 3.50	0.128 – 5.00	1.1328 – 5.00	0.997 – 5.00
0.00 – 4.00	0.118 – 5.00	1.1190 – 5.00	0.996 – 5.00
0.00 – 4.50	0.111 – 5.00	1.1109 – 5.00	1.0015 – 5.00
0.00 – 5.00	0.106 – 5.00	1.1045 – 5.00	1.003 – 5.00

Refer to Table 10. It is observed that conventional RTL inverter switches ON at an input voltage ≥ 0.6 Volts whereas Sziklai and Darlington pair RTL inverters switches ON at an input voltage ≥0.5 Volts and ≥1.0 Volts respectively. It is also apparent that, in the case of conventional RTL inverter and Sziklai pair RTL inverter, increasing the range of input pulses causes a corresponding increase in the range of output pulses in a non-linear manner. Adversely, the output pulse range of Darlington pair RTL inverter changes in zig-zag manner on increasing the range of input pulse.

3.7 Rise Time, Fall Time and Maximum Signal Frequency

In present context, the Maximum Signal Frequency describes the maximum permissible frequency of the signal than can be successfully inverted with the inverting circuit. Maximum Signal Frequency (f_{MAX}) of all the three inverters with the help of Rise Time (T_R) Fall Time (T_F) are computed using following formula and the records are listed in Table 11.

$$f_{MAX} = \frac{1}{T_R + T_F} \tag{2}$$

Table 11: Rise Time (T_R), Fall Time (T_F) and Maximum Signal Frequency (f_{MAX}) for Respective RTL Inverters

Inverters	T_R (Nano Seconds)	T_F (Nano Seconds)	$T_R + T_F$ (Nano Seconds)	f_{MAX} (Giga Hertz)
Conventional RTL Inverter	0.568	0.2719	0.8399	1.1906
Sziklai pair RTL Inverter	0.544	0.2743	0.8183	1.2220
Darlington pair RTL Inverter	0.136	0.0126	0.1486	6.7294

It is to note that the Rise Time (T_R) defines the time taken by a signal to rise from 10% to 90% of its steady-state value whereas Fall Time (T_F) measures the time that a signal takes to fall from 90% to 10% of its steady-state value [30,31].

Refer to Table 11. The Rise Time of the output pulse for Sziklai pair and Darlington pair RTL inverters is lesser than conventional RTL inverter whereas Fall Time of Sziklai pair RTL inverter is higher than other two inverters. Moreover, Conventional RTL inverter holds comparatively least amount of the f_{MAX} whereas Darlington pair RTL inverter emerges with highest value of f_{MAX}. Therefore, both the proposed inverters comparatively have a better capability to invert input signal due to higher f_{MAX} than conventional RTL inverter.

3.8 Propagation Delay Timing and Maximum Switching Frequency

Speed of the digital Inverters depends on their propagation delay time [32]. It is a parameter that measures the time an inverter takes to change its state. Ideally, it should be as short as possible. There are two types of propagation delays namely, t_{pLH} (when the output goes from LOW state to HIGH state) and t_{pHL} (when output makes a transition from a HIGH state to LOW state). The Average Propagation delay (t_p) for all the three Inverter under consideration are estimated using following formula [30,31]

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} \tag{3}$$

Where t_{pLH} and t_{pHL} are computed as follows:

High-to-Low propagation delay t_{pHL} = time taken to fall from V_{OH} to 50%.

Low-to-High propagation delay t_{pLH} = time taken to fall from V_{OL} to 50%.

In addition to it, attempt is also made to compute the Maximum Switching Frequency (f_{Smax}) of the inverters under discussion. Maximum switching frequency (f_{Smax}) is the parameter that determines the frequency at which the inverter changes its state [30,31]. It is generally determined by the following formula -

$$f_{Smax} = \frac{1}{2t_P} \tag{4}$$

The mechanism of the propagation delay timing is that when the input pulse is in the LOW state, all the transistors are treated to bear the cut-off state. Hence, no current flows across collector resistance (R_2), therefore, propagation delay time remains nil. Contrarily, when output makes a transition from LOW to a HIGH state, it does so along with a time constant whose value varies from inverter to inverter [32]. Collector resistance R_2 is also accountable for such transitions which pulls up the output from LOW to a HIGH state. Hence, it is also known as the PULL-UP resistor [32].

High-to-Low propagation delay t_{pHL}, Low-to-High propagation delay t_{pLH}, average propagation delay t_p and the Maximum Switching Frequency (f_{Smax}) are recorded in Table 12.

Table 12: Average Propagation Delay and Maximum Switching Frequency

Inverter	t_{pHL} (Nano Seconds)	t_{pLH} (Nano Seconds)	t_p (Nano Seconds)	f_{Smax} (Giga Hertz)
Conventional Inverter	0.2332	0.606	0.4196	1.1916
Sziklai Inverter	0.325	0.516	0.4205	1.1890
Darlington Inverter	0.1502	0.536	0.3431	2.1237

It is apparent from Table 12 that the propagation delay timing of respective inverters is low enough and within the permissible limit. The Darlington pair RTL inverter has the lowest propagation delay timing than Sziklai pair and Conventional RTL invertors. Moreover, the Maximum Switching Frequency of Darlington pair RTL inverter is found greater than other two inverters with Sziklai pair RTL inverter to have lowest switching frequency.

Conclusively, both Darlington pair and Sziklai pair RTL inverter circuits can be a good competitor of the Conventional RTL inverter and can successfully replicate it in switching circuits.

3.9 Variation of Output Pulse Range with Temperature

Variation of output pulse range as a function of temperature for the respective inverters are also observed and the records are displayed in Table 13. It is apparent from the table that the output pulse range of conventional RTL Inverter decreases with the rise of temperature whereas it increases with temperature elevation for Sziklai pair and Darlington pair RTL inverters. Conclusively, the lower temperature supports the performance of conventional RTL Inverter whereas Sziklai pair and Darlington pair RTL Inverters perform better at higher temperature.

Table 13: Variation of Output Pulse Range with Temperature

Temperature (ºC)	Range of Output Pulses (In Volts)		
	RTL Inverter	Sziklai Pair RTL Inverter	Darlington Pair RTL Inverter
-60	0.076 – 5.00	1.1254 – 5.00	1.0527 – 5.00
-40	0.083 – 5.00	1.1214 – 5.00	1.0420 – 5.00
-20	0.090 – 5.00	1.1168 – 5.00	1.0309 – 5.00
0	0.096 – 5.00	1.1119 – 5.00	1.0194 – 5.00
10	0.100 – 5.00	1.1092 – 5.00	1.0135 – 5.00
27	0.106 – 5.00	1.1045 – 5.00	1.0033 – 5.00
40	0.110 – 5.00	1.1008 – 5.00	0.9954 – 5.00
60	0.117 – 5.00	1.0947 – 5.00	0.9820 – 5.00

4. Conclusions

Darlington and Sziklai pairs are traditionally treated as a useful device for various amplifier designs. However, their uses in logic circuits are yet to be established. The

present manuscript, in this direction, sets a mile stone with a novel idea to observe the behaviour of Darlington and Sziklai pairs in RTL inverter (NOT Logic Circuit). Observations suggests the suitability of proposed Darlington and Sziklai pair RTL inverters for high drive current applications. Proposed inverters effectively remove the low-drive current and low static-noise-margin problem of conventional CMOS and TTL inverters. With nearly ideal switching threshold voltage of Sziklai pair RTL inverter, both the proposed inverters are capable to produce high drive current and full output swing. Proposed inverters emerge as good replicant of conventional RTL inverter in the operational temperature range $-60 \leq T \leq 60$ under 5 Volt DC biasing environment.

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