Journal of Rajasthan Academy of Physical Sciences
ISSN: 0972-6306; URL: http://raops.org.in
Vol.20, No.1&2, January-June, 2021, 119-138

NEW CIRCUIT MODEL OF SMALL-SIGNAL AMPLIFIERS WITH DARLINGTON PAIRS UNDER SZIKLAI PAIR TOPOLOGY

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Abstract: The manuscript introduces a novel idea of designing two discrete circuits of small-signal amplifiers by placing unlike Darlington pairs under Sziklai pair topology. Proposed amplifiers, named as Circuit-1 and Circuit-2, are designed and qualitatively analyzed with the aid of PSpice circuit simulation program. Circuit-1 consists of commercial models of unmatched NPN and PNP transistors to constitute Darlington pairs kept under Sziklai pair topology whereas Circuit-2 involves user-defined Spice models of matched BJTs in the device structure. Variational effect of the current gain factor β, small-signal AC equivalent circuit analysis, temperature dependency of the performance parameters and variation in phase and circuit noises at different input signal frequencies are primely discussed for the proposed amplifiers. An effort is also done to find the possibility of raising other amplifier configurations with the floated idea of circuit designing. The problem of finding matched BJTs of opposite polarity for the Sziklai pair, poor response problem of Darlington pairs at higher frequencies and narrow bandwidth problem of small-signal Sziklai pair amplifier are also addressed through the proposed designs. Circuit-1 is capable of amplifying the AC signals of 1μV-5mV range with 179.114 voltage gain, 20153 current gain and a frequency band extending from 28.341Hz to 432.125KHz. However, Circuit-2 can amplify low magnitude AC signals of 0.1μV-10mV range with 68.718 voltage gain, 716.956 current gain and a bandwidth extended from 30.580Hz to 15.163MHz. Qualitative features of both the proposed circuits suggest their possible use in submarine communication, non-directional navigational radio beacons (NDBs) for maritime and aircraft navigation and preamplifier stages of Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC) testing equipment.

Key Words: Sziklai pair, Complementary Darlington pair, Sziklai pair amplifier, Small-signal amplifier, Circuit Simulation

1. Introduction

Common Collector (CC) amplifiers generally exhibit unit voltage gain, high current gain and an input impedance much higher than output impedance and therefore it is frequently used as a voltage buffer to realize impedance matching in CRO circuit, video stage of the television receiver and voltage regulator in power supplies [8,9,12,16].

Similarly, Darlington and Sziklai Pairs are the popular device configurations for various electronics and communication circuit systems [2,4,5,6,7,10,15,16,17,18,19,21,22,23,24]. Darlington pair holds two identical transistors with the emitter of first gets connected with base of the second and both the transistors share same collector current [6,7,23]. However, Szikali pair consists of two opposite polarity transistors with the collector of first joins the base of the second [7,10,19]. Darlington and Sziklai pairs are considered complementary to each other in many applications due to the almost identical range of their current gain factor β, voltage gain, input impedance and output impedance [19,21,22]. However, due to half base turn-on voltage, low power dissipation tendency and higher switching speed, Sziklai pair, now a day, gradually replaces Darlington pair in power amplifier and digital switching type of circuits [19]. Moreover, due to better thermal stability and lower quiescent current, the Sziklai pair is also a good candidate for linear circuits [7].

Darlington pair, despite of providing poor performance at high frequencies, is a frequently used configuration to design small-signal and power amplifiers whereas the use of Sziklai pairs in the electronic industry is limited to the design of push-pull or quasi complementary symmetry type of power amplifiers [4,5,6,7,10,15,16,17,18,19,21, 22,23,24]. In recent years, some sincere efforts are being made to design small-signal amplifiers with Sziklai pair topology using CE configuration [4,7,10,20,21. Moreover, a variety of CC amplifier circuits with single BJT or paired BJTs like Darlington pair are being used by the electronic industry but the possibility of using Sziklai pair topology in CC amplifier is still a challenging dimension of research [9,12,8,5,17,2].

However, compensating the technical gap, the proposed design of CC amplifiers with a novel idea to use opposite polarity Darlington pairs under Sziklai pair topology genuinely resolve the poor response problem of small-signal Darlington pair amplifier at higher frequencies, narrow-band response problem of small-signal CE Sziklai pair amplifier and the problem of finding matched BJTs of opposite polarity for the Sziklai pair [19,7,21]. The salient feature of the proposed amplifiers is the emergence of the high voltage gain due to typical device structure along with the high current gain due to CC circuit configuration.

2. Research Method

2.1 Proposed Circuit Design

The present investigation comprises simulation and analysis of two proposed amplifiers, named as Circuit-1 and Circuit-2. Proposed amplifiers comprise similar circuit designs but having different device models with a new idea to connect two unlike Darlington pairs under Sziklai pair topology. Fig.1 describes the basic circuit design of Circuit-1 and Circuit-2 amplifiers. It is to mention that Fig.1 reflects Circuit-1 amplifier design when the device structure of the circuit uses standard commercial transistors Q2N2907A for PNP transistors Q1, Q2 and Q2N2222 for NPN transistors Q11, Q22. However, Fig.1 replicates Circuit-2 amplifier design when the device structure accommodates user-defined PSpice models of BJTs QMODP for PNP transistors Q1, Q2 and QMODN for NPN transistors Q11, Q22 [14].

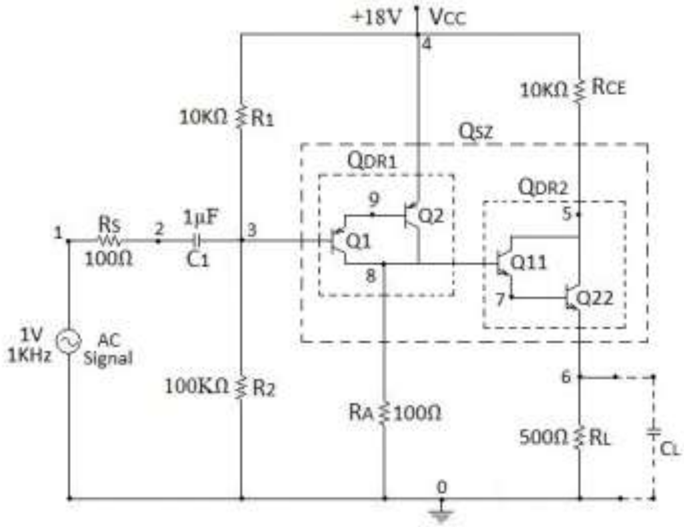

Fig.1: Basic Circuit Design of Proposed Circuit-1 and Circuit-2 amplifiers

It is also to note that transistors Q1 and Q2 in the basic circuit design (Fig.1) constitute PNP Darlington pair QDR1 whereas transistors Q11 and Q22 together form NPN Darlington pair QDR2. However, the combination of Darlington pairs QDR1 and QDR2 are placed under Sziklai pair topology to constitute a Sziklai pair QSZ [13].

As is indicated in basic design (Fig.1), placement and values of biasing resistances, capacitors, AC signal source and DC biasing supply are similar for both the proposed amplifiers (Circuit-1 and Circuit-2). Moreover, respective amplifiers acquire CC (Common Collector) topology with voltage divider biasing network [11,3].

2.2 Mode of Study

Following Fig.1, discrete designs of the proposed amplifiers, Circuit-1 and Circuit-2, are tested with the aid of PSpice simulation software [19]. Since Fig.1 designates a novel amplifier design, therefore, observational records, scripted herein, are preferred in the tabular form to cover a wide spectrum of studies and analysis. Variational effect of current gain factor, small-signal AC equivalent circuit analysis, temperature dependency of the performance parameters and variation in phase and noises with input signal frequency are the prime studies that authenticate the proposed design of Circuit-1 and Circuit-2 amplifiers.

The nucleus of the proposed circuits is the device structure, which in Circuit-1 uses commercial BJTs whereas it holds modeled BJTs in Circuit-2. PSpice model parameters related to the commercial and user-defined BJT models are listed in Table-1. To address the problem of finding matched BJTs of opposite polarity for Sziklai pairs, identical model parameters are selected to designate QMODP and QMODN transistor models of Circuit-2 [19,4,20,14].

Table 1. Model Parameters for Commercial and User-defined BJT Models

Model Parameters	Q2N2907A	Q2N2222	QMODP	QMODN
IS (p-n saturation current)	650.60E-18	14.34E-15	200.00E-18	200.00E-18
BF (Ideal maximum forward beta)	231.7	255.9	100	100
NF (Forward current emission coefficient)	1	1	1	1
VAF (Forward Early Voltage)	115.7	74.03	DEFAULT	DEFAULT
IKF (Corner for forward-beta high-current roll-off)	1.079	0.2847	DEFAULT	DEFAULT
ISE (Base-emitter leakage saturation current)	54.81E-15	14.34E-15	DEFAULT	DEFAULT
NE (Base-emitter leakage emission coefficient)	1.829	1.307	DEFAULT	DEFAULT
BR (Ideal maximum reverse beta)	3.563	6.092	1	1
NR (Reverse current emission coefficient)	1	1	1	1
RB (Zero-bios (maximum) base resistance)	10	10	5	5
RC (Collector ohmic resistance)	0.715	1	0	0
RE (Emitter Ohmic resistance)	DEFAULT	DEFAULT	0	0
CJE (Base-emitter zero-bias p-n capacitance)	19.82E-12	22.01E-12	DEFAULT	DEFAULT
MJE (Base-emitter p-n grading factor)	0.3357	0.377	DEFAULT	DEFAULT
CJC (Base-Collector zero-bias p-n capacitance)	14.76E-12	7.30E-12	DEFAULT	DEFAULT
MJC (Base-Collector p-n grading factor)	0.5383	0.3416	DEFAULT	DEFAULT
TF (Ideal forward transit time)	603.70E-12	411.10E-12	200.00E-12	200.00E-12
XTF (Transit-time bias dependence coefficient)	1.7	3	DEFAULT	DEFAULT
VTF (Transit-time dependency on V_{BC})	5	1.7	DEFAULT	DEFAULT
ITF (Transit-time dependency on Ic)	0.65	0.60	DEFAULT	DEFAULT
TR (Ideal reverse transit time)	111.30E-09	46.91E-09	5.00E-09	5.00E-09
XTB (Forward and reverse beta temperature coefficient)	1.5	1.5	DEFAULT	DEFAULT

Both the amplifiers are fed with 1V, 1KHz AC signal source but only 1mV signal strength at 1KHz frequency is provided to the respective circuits for amplification. Moreover, Circuit-1 genuinely amplifies the small input AC signals ranging in 1µV-5mV whereas this range for Circuit-2 is 0.1µV-10mV.

3. Results and Discussion

3.1. Performance Parameters

Performance parameters of the proposed amplifiers (Circuit-1 and Circuit-2) are summarized in Table 2A and Table 2B. However, Fig.2 describes the variation of the voltage gain of the proposed amplifiers with frequency whereas Fig.3 and Fig.4 depict the current gains as a function of frequency. Respective observations are recorded under two circumstances. First without considering the RMS values of the input and output signals (Table 2A) and second by taking RMS values of the respective signals into the account (Table 2B).

Table 2A. Performance Parameters of the amplifiers without RMS values

Performance Parameters without RMS Values	**Circuit-1**	**Circuit-2**
Voltage Gain A_{VG}	179.114	68.718
Upper Cut Off Frequency F_H corresponding to A_{VG}	432.154KHz	15.164MHz
Lower Cut Off Frequency F_L corresponding to A_{VG}	28.341Hz	30.580Hz
Band-Width B_W corresponding to A_{VG}	432.125KHz	15.163MHz
Current Gain A_{IG}	20153	716.956
Upper Cut Off Frequency F_H corresponding to A_{IG}	13.708KHz	9.073MHz
Current (I_{RL}) Across Load R_L	28.527mA	5.553mA
Voltage (V_{RL}) Across Load R_L	14.264V	2.776V
Power Gain (P_G) in dB $10xLog_{10}(P_O/P_I)$	123.770	79.207
Total Harmonic Distortion THD (first 10 harmonic terms)	0.888%	1.074%

Table 2B. Performance Parameters of Proposed amplifiers in terms of RMS values

Performance Parameters with RMS Values	**Circuit-1**	**Circuit-2**
Voltage Gain A_{VG-AC}	178.866	68.709
Upper Cut Off Frequency F_H corresponding to A_{VG-AC}	1.021MHz	35.568MHz
Lower Cut Off Frequency F_L corresponding to A_{VG-AC}	66.023Hz	70.987Hz
Band-Width B_W corresponding to A_{VG-AC}	1.020MHz	35.567MHz
Current Gain A_{IG-AC}	20153	716.956
Upper Cut Off Frequency F_H corresponding to A_{IG-AC}	22.959KHz	15.909MHz
RMS Value of Current (I_{RL}) Across Load R_L	28.167mA	5.416mA
RMS Value of Voltage (V_{RL}) Across Load R_L	14.083V	2.708V
Power Gain (P_{G-AC}) in dB $10xLog_{10}(P_O/P_I)$	126.345	81.673

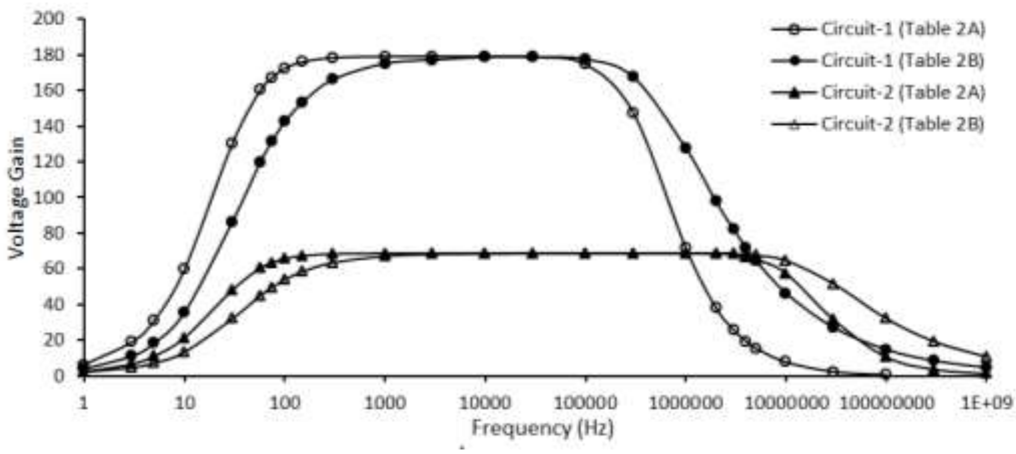

Fig.2. Variation of Voltage gain with frequency for Circuit-1 and Circuit-2

Fig.2, Fig.3, Fig.4, Table 2A and Table 2B indicate that the Voltage gain of Circuit-1 amplifier with commercial PNP and NPN BJTs are almost 2.6 times higher than Circuit-2 configuration which consists of user-defined Spice model of BJTs. The current gain of Circuit-1 is almost 28 times higher than Circuit-2 whereas the bandwidth of Circuit-2 is found to be almost 35 times wider than Circuit-1. Thus, Circuit-1 provides a higher voltage and current gains than Circuit-2 with a compromise over amplifier bandwidth. Although, Circuit-1 reflects lower THD (Total Harmonic Distortion is observed for the first 10 harmonics) than Circuit-2 but its operational input signal range (1μV-5mV) is lesser than Circuit-2 which is capable to amplify 0.1μV-10mV input signal at 1KHz operational frequency.

Respective Tables and Figures also suggest that the proposed amplifiers are free from the problem of poor response of Darlington pair amplifiers at higher frequencies and narrow bandwidth problem of small-signal Sziklai pair amplifier [10,14]. Moreover, the use of matched BJTs of opposite polarities in the device structure of Circuit-2 also resolves the problem of developing small-signal Sziklai pair amplifiers with unmatched BJTs of opposite polarity [6,19,4,22,1].

It is also to note that Emitter Follower or Common Collector configuration in small-signal amplifiers is normally used to receive high current gain with almost unity voltage gain [16,12]. However, in the present case, Circuit-1 and Circuit-2 amplifiers show Class-A amplification properties and simultaneously produce high voltage and current gains that reflect the attainment of a significant amount of the power gain with the proposed circuit designs. This feature is unique for small signal amplifiers which implies Emitter Follower topology in its circuit design as is the case with Circuit-1 and Circuit-2.

Refer to Table 2A and Table 2B. With or without taking RMS values of the input and output signals into the account, the performance parameters of respective amplifiers are found almost similar except bandwidth which shifts towards lower frequency region, if moved from Table 2A to Table 2B.

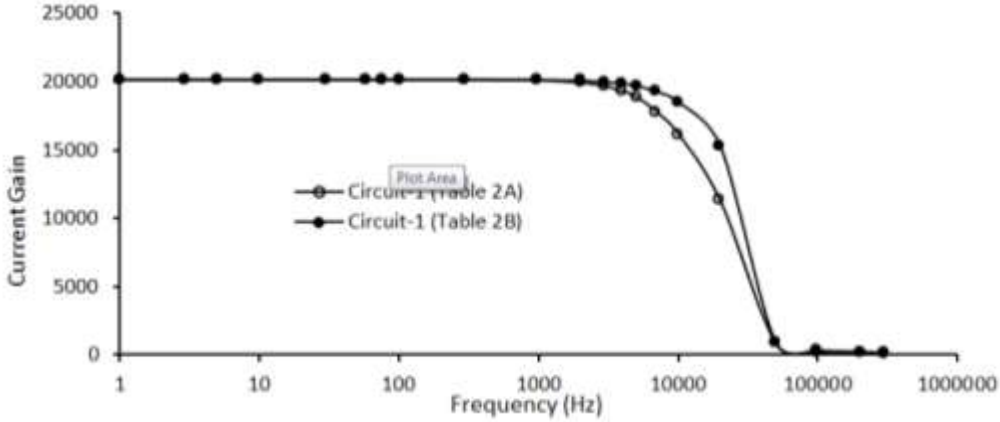

Fig.3. Current gain as a function of frequency for Circuit-1

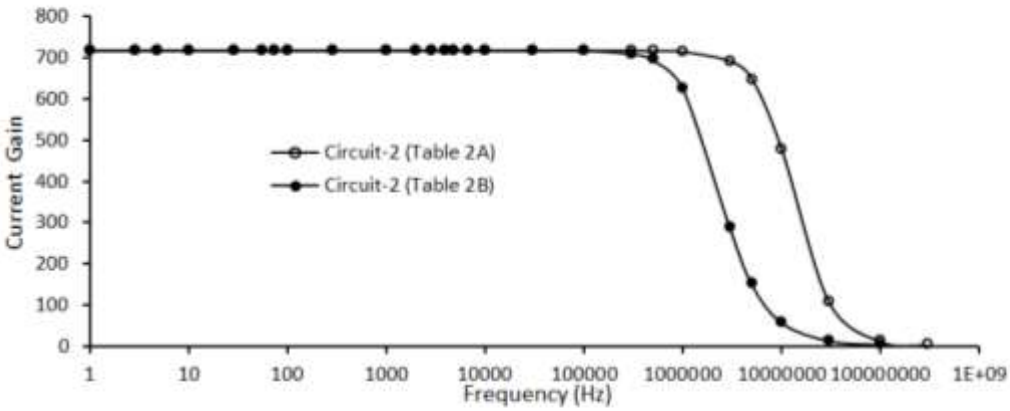

Fig.4. Current gain as a function of frequency for Circuit-2

Performance parameters in Table 2A, Table 2B and Fig.2, Fig.3, Fig.4, reflecting the qualitative features of the proposed amplifiers, indicate that the response of Circuit-1 covers Super Low Frequency (SLF) to Low Frequency (LF) range whereas the response of Circuit-2 covers the Super Low Frequency (SLF) to Medium Frequency (MF) range. This suggests that the proposed amplifier designs may be used in High-gain Low-frequency receiver applications, submarine communication, non-directional navigational radio beacons (NDBs) for maritime and aircraft navigation and preamplifier stages of Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC) testing equipment.

3.2. Effect of Beta (β) Variation

Performance parameters of the proposed Circuit-2 at different values of β are recorded in Table-3. This type of observation is not recorded for Circuit-1 because the circuit uses commercial transistors of fixed β values [14].

Table 3. Performance parameters of proposed Circuit-2 on different values of β

Performance Parameters	BETA (β) for Q1, Q2 and Q11, Q22				
	β=50	**β=100**	**β=150**	**β=250**	**β=300**
A_{VG}	33.202	68.718	108.075	177.047	207.136
F_L	91.208Hz	30.580Hz	26.670Hz	22.926Hz	21.911Hz
F_L	70.296MHz	15.164MHz	10.173MHz	6.088MHz	5.092MHz
B_W	70.295MHz	15.163MHz	10.172MHz	6.087MHz	5.091MHz
A_{IG}	269.415	716.956	1.2975K	2.4778K	3.0344K
F_H	15.760MHz	9.1819MHz	6.8814MHz	4.8504MHz	4.2694MHz
THD	1.167%	1.074%	1.066%	1.072%	1.073%

To resolve the problem of using unmatched BJTs of opposite polarity in Sziklai pairs, records in Table 3 are compiled by taking identical β values for all the four transistors Q1, Q2, Q11 and Q22 of Circuit-2 [19,4,22]. The table suggests that Circuit-2 provides faithful amplification for β values falling between 50 to 300. Moreover, both voltage and current gain increase with an elevation of β on the cost of a significant reduction in bandwidth. This probably happens because at 1KHz operating frequency, the higher β of the transistors in Circuit-2 causes a reduction in junction capacitance which interferes with the circuit performance and causes a reduction of the bandwidth. It is also observed that Circuit-2 appears with more promising features than Circuit-1 at β=250 and β=300.

3.3. Effect of Biasing Resistances and Biasing Source

The amplifier performance widely depends on the values and placement of the biasing resistances in the circuit design [11,3]. The permissible range of the biasing resistances for the faithful amplification from Circuit-1 and Circuit-2 amplifiers is listed in Table 4.

Table 4. Permissible Resistance Range for Faithful Amplification from Circuit-1 and Circuit-2

Biasing Resistances	Resistance Range for Circuit-1	Resistance Range for for Circuit-2
R_S (Input Source Biasing Resistance)	5Ω to 20KΩ	1Ω to 50KΩ
R_1 (Biasing Resistance of the Voltage Divider Network)	9KΩ to 13KΩ	10KΩ to 15KΩ
R_2 (Biasing Resistance of the Voltage Divider Network)	80KΩ to 115KΩ	90KΩ to 105KΩ
R_{CE} (Collector Biasing Resistance)	100Ω to 100KΩ	50Ω to 500KΩ
R_A(Additional Biasing Resistance)	30Ω to 20KΩ	30Ω to 900Ω
R_L (Load Resistance)	100Ω to 1KΩ	50Ω to 100KΩ

Observations based on the records of Table 4 suggests that the variation in individual biasing resistances (keeping others intact) realize a wide variation in the magnitude of performance parameters of Circuit-1 and Circuit-2 amplifiers. Just to quote, for Circuit-1 A_{VG} is observed to be 2.167 at R_A=20KΩ and 189.856 at R_L=900Ω, A_{IG} is found to be 1.113 at R_2=80KΩ and 66549 at R_L=100Ω whereas B_W is detected to be 17.10KHz at R_S=20KΩ and 1.828MHz at R_A=20KΩ. Similarly, for Circuit-2, A_{VG} is received to be

6.504 at R_S=50KΩ and 264.878 at R_A=900Ω, A_{IG} is observed to be 1.568 at R_1=15KΩ and 11498 at R_1= 11KΩ whereas B_W is found to be 13.753MHz at R_A=30Ω and 33.783 MHz at R_1=15KΩ. Thus, the variation in individual biasing resistances makes the proposed amplifiers enable to produce circumstantial performance.

In addition, it is found that Circuit-1 produces faithful amplification in the 16V to 22V range of V_{CC} whereas the permissible range of V_{CC} for Circuit-2 extends from 17V to 20V. It is also to note that the voltage and current gains of Circuit-1 decrease for higher or lower values of V_{CC} other than 18V whereas voltage and current gains of Circuit-2 decrease for V_{CC}< 20V.

3.4. Effect of Capacitors

Capacitors C_1 and C_L in circuit design (Fig.1) of the proposed amplifiers Circuit-1 and Circuit-2 draw significant impact on the performance parameters [11,3]. Respective observations at different permissible values of C_1 for Circuit-1 and Circuit-2 are recorded in Tables 5A and 5B whereas those for Circuit-2 are listed in Tables 6A and 6B.

Refer to Table 5A and Table 5B. The permissible range of C_1 for the faithful amplification by proposed circuits extends from 0.01μF to 50μF. It is also to note that variation of C_1 in Circuit-1 does not alter the current gain of the amplifier system whereas voltage gain improves with increasing C_1 but this increase in voltage gain is marginal for C_1≥1μF. However, bandwidth decreases with rising values of C_1 for Circuit-1 with a significant shift towards the lower frequency region. Similarly, a variation of C_1 in Circuit-2 does not alter the value of the current gain. However, for Circuit-2, the voltage gain increases with rising C_1 but acquires constancy level for C_1>1μF whereas bandwidth is also found to have a shifting tendency towards lower frequency region.

Table 5A. Performance Parameters of Circuit-1 at different values of C_1

Capacitance C_1	Circuit-1 Current Response		Circuit-1 Voltage Response				THD %
	A_{IG}	F_H	A_{VG}	F_L	F_H	B_W	
0.01μF	20153	13.434KHz	148.277	2.336KHz	526.599KHz	526.596KHz	2.072%
0.1μF	20153	13.456KHz	175.790	279.692Hz	443.420KHz	443.140KHz	1.260%
1μF	20153	13.708KHz	179.114	28.341Hz	432.154KHz	432.125KHz	0.888%
10μF	20153	13.452KHz	179.453	2.834Hz	432.227KHz	432.224KHz	0.868%
50 μF	20153	13.380KHz	179.483	0.570Hz	432.473KHz	431.903KHz	0.864%

Table 5B. Performance Parameters of Circuit-2 at different values of C_1

Capacitance C_1	Circuit-2 Current Response		Circuit-2 Voltage Response				THD %
	A_{IG}	F_H	A_{VG}	F_L	F_H	B_W	
0.01μF	716.956	9.1080MHz	68.688	3.041KHz	15.237MHz	15.236MHz	2.214
0.1μF	716.956	9.1324MHz	68.716	30.334Hz	15.180MHz	15.179MHz	1.456
1μF	716.956	9.0730MHz	68.718	30.580Hz	15.164MHz	15.163MHz	1.074
10μF	716.956	9.1485MHz	68.719	3.054Hz	15.213MHz	15.212MHz	1.054
50 μF	716.956	9.1380MHz	68.719	0.599Hz	15.124MHz	15.123MHz	1.051

Similarly, Tables 6A and 6B refer that the permissible range of C_L for the faithful amplification extends from 0.01μF to 100μF for Circuit-1 and 0.0001μF to 50μF for Circuit-2. It is to note that variation of C_L in respective amplifiers do not alter the current gain of the amplifier system whereas voltage gain decreases with increasing C_L but this decrement in voltage gain is marginal for $C_L \leq 0.1$μF. In addition to it, the bandwidth of voltage gain and current gain responses also decreases with rising values of C_L for Circuit-1 and Circuit-2 with a significant shift towards the lower frequency region.

Table 6A. Performance Parameters of Circuit-1 at different values of Load Capacitor C_L

Capacitance C_L	Circuit-1 Current Response		Circuit-1 Voltage Response				THD %
	A_{IG}	F_H	A_{VG}	F_L	F_H	B_W	
0.01μF	20153	12.785KHz	179.092	28.395Hz	148.698KHz	148.669KHz	1.338
0.1μF	20153	8.483KHz	178.870	28.297Hz	19.748KHz	19.719KHz	0.786
1μF	20153	1.819KHz	176.681	27.719Hz	2.077KHz	2.049KHz	0.244
10μF	20153	203.658Hz	157.435	23.111Hz	252.684Hz	229.573Hz	1.672
50μF	20153	41.137Hz	105.913	13.937Hz	82.783Hz	68.846Hz	3.290
100μF	20153	20.589Hz	75.438	9.804Hz	58.081Hz	48.277Hz	3.360

Table 6B. Performance Parameters of Circuit-2 at different values of Load Capacitor C_L

Capacitance C_L	Circuit-2 Current Response		Circuit-2 Voltage Response				THD %
	A_{IG}	F_H	A_{VG}	F_L	F_H	B_W	
0.0001μF	716.956	7.7056MHz	68.718	30.026Hz	10.302MHz	10.301MHz	1.075
0.001μF	716.956	1.6242MHz	68.717	30.151Hz	1.6693MHz	1.6692MHz	1.082
0.01μF	716.956	168.500KHz	68.706	30.522Hz	163.501KHz	163.470KHz	1.065
0.1μF	716.956	16.977KHz	68.592	30.197Hz	16.969KHz	16.938KHz	0.981
1μF	716.956	1.691KHz	67.485	29.510Hz	1.757KHz	1.727KHz	0.378
10μF	716.956	169.418Hz	58.121	23.037Hz	222.717Hz	199.680Hz	2.223
50μF	716.953	33.896Hz	36.223	13.569Hz	77.640Hz	64.071Hz	4.880

Refer to Tables 5A, 5B, 6A and 6B. It is to note that the behaviour of Circuit-1 and Circuit-2 for $C_1 \geq 1$μF leads to the tunning facility to the respective amplifiers [22,1,20]. Changes in C_1 for $C_1 \geq 1$μF do not affect voltage and current gain but forces bandwidth to shift towards lower frequency region, thus may play a significant role to adjust frequency bandwidth and therefore provide the tunning facility. Circuit-1 and Circuit-2 also show similar behaviour for $C_L \leq 0.1$μF.

3.5. Small-Signal AC Equivalent Circuit

Small-signal AC equivalent circuit corresponding to the basic design of proposed amplifiers (Fig.1) is sketched in Fig.5 with consideration that coupling and bypass capacitors act as short circuit at mid and high frequencies and do not significantly affect the amplifier performance [13]. Parasitic capacitances are also ignored in the equivalent circuit to overcome the complexity of the analysis.

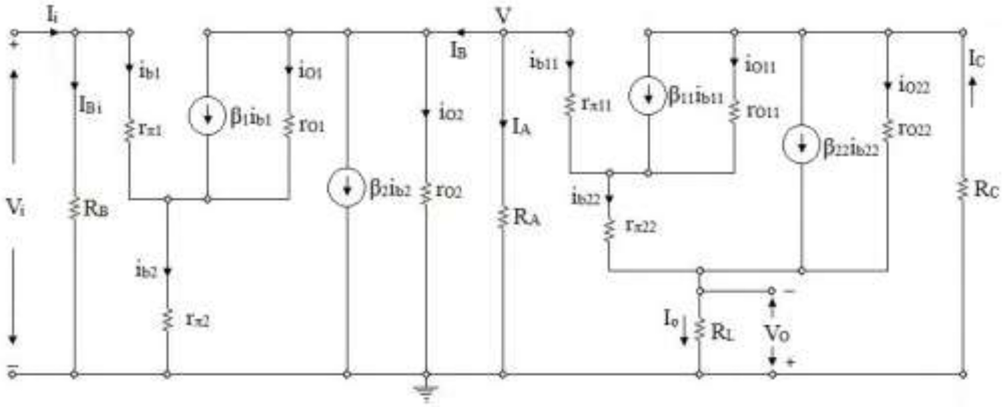

Fig.5. Small-signal equivalent circuit of the proposed amplifiers

It is to mention that simulation of the Circuit-1 amplifiers leads to β_1=219, β_2=199, β_{11}=-0.994, β_{22}=176, $r_{\pi 1}$=6.27x10$^3\Omega$, $r_{\pi 2}$=27.8Ω, $r_{\pi 11}$=34.6Ω, $r_{\pi 22}$=172Ω, r_{O1}=1.25x10$^5\Omega$, r_{O2}=629Ω, r_{O11}=0.223Ω and r_{O22}=2.64x10$^3\Omega$. Similarly, the simulation of Circuit-2 amplifier leads to β_1=100, β_2=100, β_{11}=-0.986, β_{22}=100, $r_{\pi 1}$=5.60x10$^3\Omega$, $r_{\pi 2}$=55.4Ω, $r_{\pi 11}$=657Ω, $r_{\pi 22}$=483Ω, r_{O1}=1.00x10$^{12}\Omega$, r_{O2}=1.00x10$^{12}\Omega$, r_{O11}=6.59Ω and r_{O22}=9.92x10$^{11}\Omega$. Since r_{O1}, and r_{O22} in both the proposed circuits are large and the parallel combination of R_A and r_{O2} reflects the resistance value approximately equal to R_A. This provides sufficient ground to ignore r_{O1}, r_{O2} and r_{O22} in Fig.5 and to obtain the reduced equivalent circuit as depicted in Fig.6 for the analysis purpose.

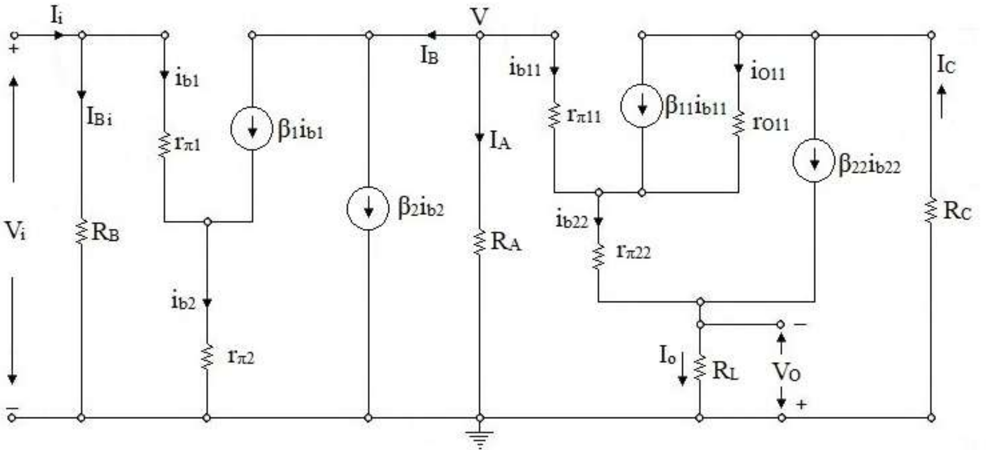

Fig.6. Reduced small-signal equivalent circuit of the proposed amplifiers

The basic circuit equations for Fig.6 can be framed as follows -

$$i_{b22} = i_{b11} + \beta_{11} i_{b11} + i_{O11} = i_{b11}(1 + \beta_{11}) + i_{O11}$$

$$I_C = i_{O11} + \beta_{22} i_{b22} + \beta_{11} i_{b11} \quad (1)$$

$$I_C R_C = i_{O11} r_{O11} + i_{b22} r_{\pi 22} + I_O R_L \quad (2)$$

$$i_{b11} = -(I_A + I_B) \quad (3)$$

$$I_B = \beta_1 i_{b1} + \beta_2 i_{b2} \quad (4)$$

$$i_{b2} = i_{b1} + \beta_1 i_{b1} = i_{b1}(1 + \beta_1) \quad (5)$$

$$V_i = I_{Bi} R_B = i_{b1} r_{\pi 1} + i_{b2} r_{\pi 2} \quad (6)$$

$$I_i = I_{Bi} + i_{b1} \quad (7)$$

$$I_O = i_{b22} + \beta_{22} i_{b22} = i_{b22}(1 + \beta_{22}) \quad (8)$$

$$V = I_A R_A \quad (9)$$

$$V = i_{b11} r_{\pi 11} + i_{b22} r_{\pi 22} + V_O \quad (10)$$

$$V_O = I_O R_L \quad (11)$$

Based on the above equations, an expression for the voltage gain A_V of the proposed amplifier circuits (Circuit-1 and Circuit-2) can be deduced as follows -

$$A_V = \frac{-\{\beta_1+\beta_2+\beta_1\beta_2\}[(1+\beta_{11})(1+\beta_{22})[X]+(1+\beta_{22})[Y]]R_A R_L}{[r_{\pi 1}+(1+\beta_1)r_{\pi 2}][R_A[X]+[Z][X]+[Y][r_{\pi 22}+R_L(1+\beta_{22})]]} \quad (12)$$

Where, $[X] = [(1+\beta_{22})(R_C - R_L) - (r_{O11} + r_{\pi 22})]$ (13)

$[Y] = [(1+\beta_{11})\{r_{\pi 22} + R_L(1+\beta_{22})\} - R_C(\beta_{11} + \beta_{22} + \beta_{11}\beta_{22})]$ and (14)

$[Z] = \{r_{\pi 11} + (1+\beta_{11})[r_{\pi 22} + R_L(1+\beta_{22})]\}$ (15)

Similarly, the following expression for the current gain A_I of Circuit-1 and Circuit-2 can be obtained -

$$A_I = \frac{-\{\beta_1+\beta_2+\beta_1\beta_2\}\{(1+\beta_{11})(1+\beta_{22})[X]+(1+\beta_{22})[Y]\}R_A}{\left[1+\frac{r_{\pi 1}+(1+\beta_1)r_{\pi 2}}{R_B}\right]\{R_A[X]+[Z][X]+[Y][r_{\pi 22}+R_L(1+\beta_{22})]\}} \quad (16)$$

Where $R_B = R_1 \| R_2$

The expression for the input impedance Z_I of the proposed amplifier circuits can be obtained as given below -

$$Z_I = \frac{[r_{\pi 1}+(1+\beta_1)r_{\pi 2}]R_B}{\{R_B+[r_{\pi 1}+(1+\beta_1)r_{\pi 2}]\}} \quad (17)$$

Similarly, an expression for the output impedance Z_O of the proposed amplifier circuits can be obtained as follows -

$$Z_O = R_L \quad (18)$$

3.6. Temperature Effect on Performance Parameters

Environmental temperature draws a significant impact on the performance of amplifiers [20]. The effect of temperature on the performance of Circuit-1 and Circuit-2 is recorded in Tables 7A and 7B. Information in Table 7A indicates that Circuit-1 provides faithful amplification in -30°C to +30°C temperature range whereas Circuit-2 performs seamlessly in the temperature of -5°C to +30 °C. It is also observed by Table 7A that the voltage and current gain of Circuit-1 increases with rising temperature up to 27°C and thereafter starts decreasing. However, the bandwidth of Circuit-1 is found maximum at -20°C and below this temperature, it drops significantly whereas at temperatures higher than -20°C it has a decreasing tendency. A similar nature is found with THD except it has the highest percentage at +30°C. On the other hand, voltage and current gains of Circuit-2 have a rising tendency but THD has a decreasing tendency with temperature elevation. However, the bandwidth of Circuit-2 is found maximum at +10°C and below or above this critical temperature it has a decreasing tendency.

3.7 Variation of Parameters

Table 7A. Performance Parameters of Circuit-1 at different Temperatures

Temperature (°C)	A_{VG}	A_{IG}	F_L	F_H	B_W	THD
-30	35.686	588.304	19.184Hz	517.086KHz	517.066KHz	1.283%
-20	52.181	815.162	20.424Hz	1.636MHz	1.635MHz	1.133%
-10	80.559	1179.8	21.849Hz	1.378MHz	1.377MHz	1.050%
0	111.110	1515.4	23.435Hz	1.195MHz	1.194MHz	0.973%
+10	140.419	1779.7	25.098Hz	977.198KHz	977.172KHz	0.947%
+20	165.329	1950.4	27.215Hz	709.192KHz	709.164KHz	0.910%
+27	179.114	20153	28.341Hz	432.154KHz	432.125KHz	0.888%
+30	169.567	629.865	86.985Hz	236.053KHz	235.966KHz	5.800%

Table 7B. Performance Parameters of Circuit-2 at different Temperatures

Temperature (°C)	A_{VG}	A_{IG}	F_L	F_H	B_W	THD
-5	21.369	306.077	22.287Hz	13.827MHz	13.826 MHz	2.796%
0	34.699	474.367	23.345Hz	15.223MHz	15.222 MHz	1.288%
+10	41.273	510.953	26.087Hz	15.805MHz	15.804 MHz	1.230
+20	57.550	643.684	28.678Hz	15.232MHz	15.231 MHz	1.096
+27	68.718	716.956	30.580Hz	15.164MHz	15.163MHz	1.074%
+30	73.569	745.580	31.408Hz	15.127MHz	15.126MHz	1.067%

3.8. Temperature Effect on Input/Output Noise

Due to the distinct behaviour of active and passive components, the electronic circuits at different frequencies and temperatures, generate noises in input and output sections [8,18,20]. Input and Output noises for the Circuit-1 and Circuit-2 amplifiers at operating frequency 1KHz, lower frequency 100Hz and higher frequency 10KHz are recorded in Tables 8A and 8B respectively.

Table 8A. Variation of Circuit-1 Input and Output Noises with temperature

Temperature (^{O}C)	100Hz		1KHz		10KHz	
	Output Noise (V/Hz)	Input Noise (V/Hz)	Output Noise (V/Hz)	Input Noise (V/Hz)	Output Noise (V/Hz)	Input Noise (V/Hz)
-30	1.061E-07	3.028E-09	7.873E-08	2.207E-09	7.838E-08	2.197E-09
-20	1.490E-07	2.914E-09	1.016E-07	1.947E-09	1.010E-07	1.935E-09
-10	2.291E-07	2.911E-09	1.453E-07	1.804E-09	1.441E-07	1.789E-09
0	3.215E-07	2.971E-09	1.917E-07	1.726E-09	1.899E-07	1.709E-09
+10	4.183E-07	3.071E-09	2.369E-07	1.688E-09	2.342E-07	1.668E-09
+20	5.101E-07	3.196E-09	2.765E-07	1.673E-09	2.729E-07	1.651E-09
+27	5.674E-07	3.292E-09	2.993E-07	1.672E-09	2.950E-07	1.647E-09
+30	4.300E-07	3.339E-09	2.828E-07	1.674E-09	2.794E-07	1.648E-09

Table 8B. Variation of Circuit-2 Input and Output Noises with temperature

Temperature (^{O}C)	100Hz		1KHz		10KHz	
	Output Noise (V/Hz)	Input Noise (V/Hz)	Output Noise (V/Hz)	Input Noise (V/Hz)	Output Noise (V/Hz)	Input Noise (V/Hz)
-5	6.505E-08	3.118E-09	4.439E-08	2.078E-09	4.412E-08	2.065E-09
0	1.046E-07	3.094E-09	6.775E-08	1.953E-09	6.726E-08	1.938E-09
+10	1.260E-07	3.152E-09	7.537E-08	1.827E-09	7.464E-08	1.809E-09
+20	1.809E-07	3.269E-09	1.011E-07	1.758E-09	9.994E-08	1.737E-09
+27	2.216E-07	3.372E-09	1.188E-07	1.730E-09	1.172E-07	1.705E-09
+30	2.400E-07	3.419E-09	1.266E-07	1.721E-09	1.248E-07	1.696E-09

Observations in Tables 8A and 8B suggests that the input and output noises in respective amplifiers are low enough, indicating the fine quality of amplification. It is also observed by Table 8A that the output noise of Circuit-1 amplifier at all the recorded frequencies increases with temperature up to 27^{o}C then acquire a decreasing tendency whereas input noise at 100Hz increases continuously with temperature and at 1KHz and 10KHz frequencies, it increases up to 27^{o}C, thereafter acquires a decreasing tendency. However, Table 8B shows that the respective noises in the case of Circuit-2 increase with temperature except input noises at 1KHz and 10KHz frequencies which has a decreasing tendency with the temperature elevation.

3.9. Configurations other than the Proposed Circuits

During the exploration of the proposed amplifiers (Circuit-1 and Circuit-2) the basic circuit configuration of Fig.1 is also converted to realize four different device combinations of Darlington pairs kept under Sziklai pair topology. Respective configurations are mentioned herein as Case-1, Case-2, Case-3, Case-4 and Case-5.

When Q1 and Q2 of the PNP Darlington pair are chosen as user-defined PSpice models of PNP transistor QMODP whereas Q11 and Q22 of the NPN Darlington pair as commercial NPN transistors Q2N2222, the circuit configuration of Fig.1 designate Case-1 amplifier design.

If Q1 and Q2 of the PNP Darlington pair are chosen as commercial PNP transistors Q2N2907A and Q11 and Q22 as user-defined Spice models of NPN transistors QMODN, the circuit configuration of Fig.1 represents Case-2 amplifier design.

When in Fig.1 circuit design, Q1 is chosen as commercial PNP transistor Q2N2907A, Q2 as user-defined Spice model of PNP transistor QMODP, Q11 as commercial NPN transistor Q2N2222 and Q22 as a user-defined model of NPN transistor QMODN, the circuit configuration (Fig.1) represents Case-3 amplifier design.

When Q1 is chosen as user-defined Spice model of PNP transistor QMODP, Q2 as commercial PNP transistor Q2N2907A, Q11 as a user-defined model of NPN transistor QMODN and Q22 as commercial NPN transistor Q2N2222, the circuit configuration of Fig.1 represents Case-4 amplifier design.

Table 9. Performance parameters for the Case-1, Case-2, Case-3 and Case-4 Circuits

Performance Parameters	**Case-1**	**Case-2**	**Case-3**	**Case-4**
Maximum Voltage Gain A_{VG}	68.197	180.700	128.124	134.710
Upper Cut Off Frequency F_H	15.434MHz	434.740KHz	2.2893MHz	1.5102MHz
Lower Cut Off Frequency F_L	29.980Hz	28.825Hz	28.560Hz	30.680Hz
Band-Width B_W	15.433MHz	434.711KHz	2.2892MHz	1.51016MHz
Maximum Current Gain A_{IG}	711.515	2.0332K	1.4436K	1.3953K
Upper Cut Off Frequency F_H	9.246MHz	13.450KHz	51.866KHz	1.1417MHz
Peak Output Current (I_{RL}) Across Load R_L	5.8012mA	28.470mA	13.273mA	16.364mA
Peak Output Voltage (V_{RL}) Across Load R_L	2.900V	14.236V	6.6368V	8.1817V
Total Harmonic Distortion THD (first 10 harmonic terms)	1.073%	0.888%	1.024%	0.936%
Input Signal Voltage used for present observations (V_I)	1mV, 1KHz	1mV, 1KHz	1mV, 1KHz	1mV, 1KHz

The performance parameters defining the qualitative properties of Case-1, Case-2, Case-3 and Case-4 circuit configurations are listed in Table-9. When records of Table 9 are compared with the observations in Table 2A, the Case-1 circuit seems to have qualitative properties more or less like proposed Circuit-2 and therefore follow a similar arena of application. However, the qualitative properties of Case-2 design fall in the close vicinity of proposed Circuit-1 with a better amount of Voltage gain and bandwidth and therefore have almost similar application range. The behaviour of Case-1 and Case-2 amplifier designs infers that the Darlington pair at driver position in Sziklai pair topology of Fig.1 circuit design sets the basic behaviour of the amplifier and this is why Case-1 and Case-2 amplifiers own a qualitative property near to the proposed Circuit-2 and Circuit-1 respectively.

On the other hand, unlike BJTs in Case-3 and Case-4 amplifier designs are not exactly forming the Darlington pairs (which uses like BJTs in the device structure), instead, they are kept under Darlington pair topology and the final structure of the PNP and NPN transistor pairs with unlike BJTs are placed in Sziklai pair topology and therefore the respective circuit designs witnesses a performance deviated from Circuit-1 and Circuit-2.

3.10. Phase Variation

The phase difference between output and input signal for Circuit-1 and Circuit-2 and their sprouting configurations referred to as Case-1, Case-2, Case-3 and Case-4, is recorded on different values of operational frequency and respective observations are listed in Table 10. It is observed that approximately 180^o out of phase output is received for the initially taken operational frequency 1KHz and the next level 10KHz for all the circuit configurations, listed in Table 10. It is also observed that approximately 180^o out of phase output at 100KHz operational frequency is received for all the configurations mentioned in Table 10 except Circuit-1 and Case-2 configurations. However, Circuit-2 and Case-1 configurations provide approximately 180^o out of phase output even at 1MHz operational frequency.

It is worth noting that the typical Emitter Follower small-signal amplifier is known for 0^o input-output phase difference [16,2]. However, for the proposed design of Circuit-1 and Circuit-2 and for their sprouting configurations Case-1, Case-2, Case-3 and Case-4, which follow the Emitter Follower topology, the input-output phase relationship possesses a phase difference ranging approximately between -109^o to -300^o at different operational frequencies. Thus, perhaps due to typical device structure, the phase relationship of the referred configurations finds a close resemblance with Common Emitter small-signal amplifiers.

Table 10. Phase status of Output Signal for the circuits under discussion

Frequency of the input signal	**Phase difference recorded for Output Voltage (V_O)**					
	Circuit-1	**Circuit-2**	**Case-1**	**Case-2**	**Case-3**	**Case-4**
10 Hz	-109.468	-108.148	-108.148	-109.468	-109.493	-108.025
100 Hz	-164.216	-163.034	-163.034	-164.216	-164.227	-162.921
1 KHz	-178.511	-178.256	-178.255	-178.512	-178.407	-178.277
10 KHz	-181.157	-179.862	-179.852	-181.159	-180.085	-180.196
100 KHz	-192.956	-180.355	-180.256	-192.971	-182.453	-183.699
1 MHz	-247.021	-183.718	-183.484	-247.063	-203.559	-212.981
10 MHz	-273.501	-212.944	-213.116	-273.454	-259.198	-260.355
100 MHz	-300.562	-259.903	-260.199	-300.340	-280.598	-262.429

4. Conclusion

A common design for two small-signal amplifiers (named Circuit-1 and Circuit-2) is developed with a novel approach to place unlike Darlington pairs under Sziklai pair topology. Circuit-1 uses commercial NPN and PNP transistors to constitute the device model holding Darlington pairs under Sziklai pair topology whereas Circuit-2 involves user-defined Spice models of matched BJTs in the device structure.

The overall circuit design uses Common Collector biasing topology and therefore the respective amplifiers prominently produce high current gain. The added feature of both the proposed amplifiers is the production of high-level voltage gain with low harmonic distortion and low input and output noises in the operational temperature range. Circuit-1 provides the best results in $-30^{o}C$ to $+30^{o}C$ temperature range whereas this range for Circuit-2 extends from $-5^{o}C$ to $+30\,^{o}C$.

The proposed design provides a sincere solution to the poor response problem of Darlington pair amplifiers at higher frequencies, the narrow bandwidth problem of small-signal Sziklai pair amplifier and the problem of using unmatched BJTs of opposite polarity in Sziklai pairs.

Circuit-2 provides genuine amplification with well-matched BJTs having β values in the range 50 to 300. The study of Phase variation concludes the preferable range of operational for Circuit-1 extends from 1KHz to 10KHz whereas for Circuit-2 it spans from 1KHz to 1MHz. The tunning facility may also be availed for both the amplifiers with appropriate variation in C_1 and C_L.

The permissible input AC signal range and the bandwidth picture of both the amplifiers suggest their possible use in submarine communication, non-directional navigational radio beacons (NDBs) for maritime and aircraft navigation and preamplifier stages of Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC) testing equipment.

Acknowledgement: The authors are thankful to the Referee for valuable comments and suggestions.

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